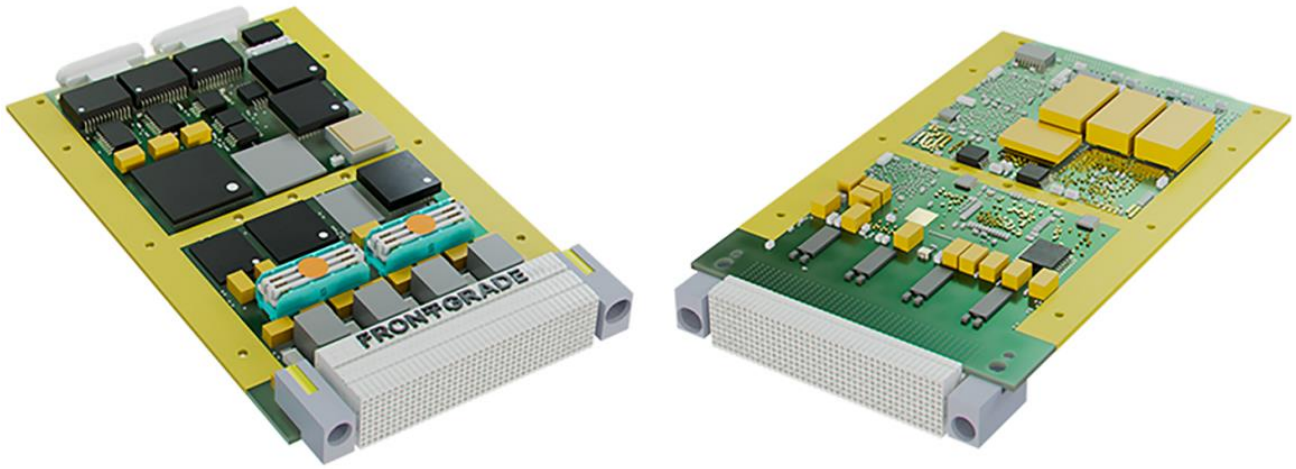
FRONTGRADE

ADV DATASHEET

UTSBC08-PS

Generation 8 SpaceVPX Single Board Computer

12/13/2024
Version #: 1.0



Introduction

The Frontgrade™ SBC8 Single Board Computer is a perfect mix of high-performance processing, interface flexibility, and low power, in a SWaP optimized design that is ideal for your space processing or C&DH needs now and into the future. This compact 3U SpaceVPX design is small, lightweight, and power efficient while offering the processing power and flexibility you need to succeed in today's competitive space markets. The SBC8 supports both the SpaceVPX System Controller and Payload module profiles:

- System Controller Slot Profile: SLT3-CON-8T-14.6.2 / Payload Module Profile: MOD3-CON-8T8U-16.6.2-1-16.12)

The Frontgrade SBC8 design features the latest Radiation Hardened and field tested Quad Core LEON4FT SPARC V8 processor (GR740) that provides up to 1800 DMIPS of processing power and pairs that with our latest Low Power, High Performance Radiation Tolerant CertusPro-NX-RT FPGA. SBC8 provides 512MB of Reed-Solomon EDAC protected SDRAM directly connected to the GR740 processor along with 256MB Dual-QSPI MRAM - providing directly connected persistent RAM storage to user applications. Additional 512MB-1GB of local expansion persistant-RAM (MRAM) is available via PCI DMA transactions from the GR740 through the Frontgrade CertusPro-NX-RT FPGA. All told, the SBC8 implements a robust memory architecture based on highly reliable, space assured, memories yielding a total of 512MB volatile SDRAM and up to 1.25GB of non-volatile MRAM. SBC8 also optionally includes up to 171GB of EDAC Corrected Non-Volatile User Data Storage.

Additionally, SBC8 features a VITA 88.0 XMC+ Mezzanine interface to allow you to use the same base SBC for all your missions but have the flexibility to add custom mezzanine CCAs to tailor front panel interfaces and processing to each individual mission's requirements. This not only allows for the flexibility you need but allows for reuse of your valuable software code base as you move from mission to mission.

To collect and report telemetry as well as oversee the major components of the design and allow for implementation of additional radiation mitigation and error handling strategies, the SBC8 includes a Radiation Hardened ARM Cortex M0+ based Microcontroller with its own independent boot and application Flash Memory.

Finally, a development "Dongle" is available to access the JTAG resources of the MCU, FPGA, and Processor as well as providing Ethernet or SpW Debug capabilities for your software development team.

Features

Performance

- GR740 Quad Core Radiation Hardened SoC from Industry Leader Frontgrade Gaisler
  - 2MB Level2 cache SDRAM Interface
  - High Speed Processing up to 1800 DMIPS (250MHz system clock @ 1.84DMIPS/MHz/Core)
  - Excellent Fight Heritage and Code Base
  - SW Compatibility: VxWorks, Linux, RTEMS
  - JTAG, Ethernet and SpaceWire debug links with GRMON and TSIM3 capabilities
- State of the art Radiation Tolerant, Low Power, High Performance FPGA used for IO and Memory expansion.
- Independent Rad Hard MCU to monitor Processor, FPGA, and board health as well as control resets, power sequencing and boot image selection.
  - Supports advanced upset and error mitigation strategies

Memory

Customize the SBC8 Memory Configuration to your specific needs with options of 512MB or 1GB of FPGA connected MRAM and the option to include 171GB of NAND Flash with BCH EDAC.

- 512MB of EDAC Corrected SDRAM
- 128KB SEU Immune MRAM (Processor Boot Memory)
- 256MB QSPI MRAM with ECC (FPGA Boot and App Storage)
- 512MB or 1GB of High Speed, Non-Volatile, 32-bit Parallel MRAM with ECC accessible over PCI from the CPU
- Up to 171GB of ECC Corrected User Accessible Non-Volatile Memory (NAND)

Front Panel Interfaces

The SBC8 Front Panel offers options of SpW, Ethernet, UART, or CAN interfaces for communications to the Spacecraft Bus and other devices as well as PPS and GPS clock inputs for mission synchronization.

- 2x SpW
- 3x 10/100/1000Base-T Ethernet Ports
  - 2x FPGA connected with 1 that also operates as an Ethernet Debug Port
  - 1x CPU connected (user + debug)
- 2x RS-422 UARTs
- 2x CAN
- PPS Input (RS-422)

Backplane Panel Interfaces

SBC8 is primarily targeted for use as a System Controller, so it adheres to a SpaceVPX Controller Backplane profile, but can be used as a payload module with all the available Backplane IO.

- 8x SpW
- 4 lanes multi-purpose SERDES (6.25Gbps)
- 2 lanes of SGMII SERDES
- 8x I2C for IPMB
- 8x Slot Resets for other boards in the chassis
- 4x PPS Outputs
- 4x 100MHz Sync Clk Outputs (can come from on board clock or GPS Reference clock implemented on a Mezannine)
- PCIe 100MHz Clk Output
- 12V Power Input (with optional 3.3V Aux usage)

Mezzanine Interfaces

A distinguishing feature of the SBC8 is its ability to adapt to your specific mission via custom mezzanines. Gone are the days of needing new SBC designs for every mission. Instead, maintain the same base SBC allowing maximum reuse of your investment in software and add features you need to make the next mission a success.

- PCI
- 4 lanes multi-purpose SERDES (6.25Gbps)
- SpW (can also be used as 4x LVDS GPIO or 8 SE GPIO)
- 1x GR740 GPIO
- PPS to/from Mez
- 4x Differential 100MHz Sync Clk from Mez + 1x Differential from Mez to Clock Network Manager
- 50MHz, 100MHz and 125MHz Clocks to Mez
- Mezzanine JTAG (to program FPGAs on Mez) – can be used as GPIO

Software & Firmware

The SBC8 is delivered with a fully tested FPGA firmware package enabling the customer choice of standard interfaces from those available. Source Code along with the Gaisler GRLIB IP Core Library is available under license. (See Ordering Options)

SBC8 is also delivered with a Linux or RTEMs BSP and Demonstration Application. Other software options (e.g. VxWORKs BSP and GRBOOT) can be delivered under license (See Ordering Options).

Developers will also have SBC8 support in the FG Gaisler TSIM3 and GRMON development tools.

Mass & Thermal

- Mass: <0.65kg, standard 3U VPX form factor
- -25°C to +65°C operational
- Power consumption: 12.8W Typical

Block Diagram

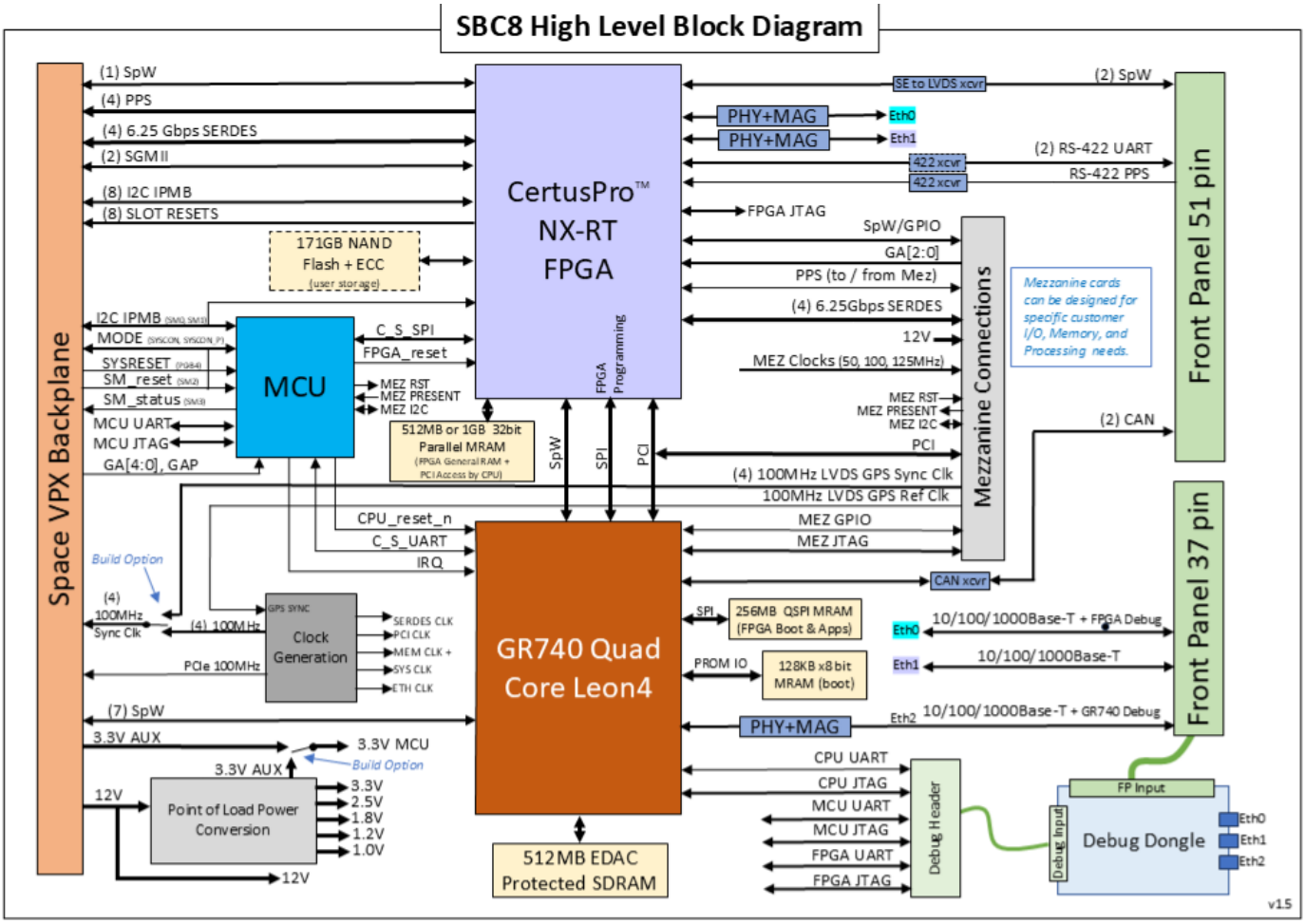


Figure 1. SBC8 High Level Block Diagram

Standard Hardware and Firmware Build

(Referenced to Ordering Information)

The standard build consumes the following percentages of the CertusPro-NX FPGA resources:

- LUT4% = 79%
- Registers = 37%
- Embedded Block RAM = 85%

Front Panel Connections to CertusPro-NX FPGA

- 2x 1000Base-T Ethernet
- 2x SpW Ports
- 2x RS-422 UARTs
- 0x CAN
- 1x PPS Input

XMC+ Mezzanine Connections to CertusPro-NX FPGA

- 1x PCI (shared with PCI to GR740)
- 0x SpW – (wired in hardware, but not implemented in standard firmware build)
- 0x SERDES (6.25Gbps) – (wired in hardware, but not implemented in standard firmware build)
- 0x GA Inputs – (wired in hardware, but not implemented in standard firmware build)
- 1x PPS Output

Backplane Connections to CertusPro-NX FPGA

- 1x SpW Port
- 2x Lanes multi-purpose SERDES (6.25Gbps)
- 1x Lane SGMII Serdes
- 4x I2C for IPMB
  — Includes 4x GPIO Reset for other boards in the chassis
- 4x PPS Outputs (LVDS)

Other Functions in CertusPro-NX FPGA

- 1x PCI Target for GR740
- 1x SpW to GR740
- 1x SPI FPGA Programming Interface
- 1x Parallel MRAM Interface (512GB)
- 0x NAND Flash Controller
- 1x AHB RAM (128)
- 2x Lanes multi-purpose SERDES (6.25Gbps)

Interfaces

The SBC8 provides two front panel connectors (51 pin and 37 pin), an XMC+ mezzanine connection, and a SpaceVPX backplane interface. The interfaces and pinouts are described below.

J3: 51-pin Front Panel Connector

Table 1. J3 Connector Pinlist

J3 – Connector Pinlist for SpaceWire, CAN Bus, RS-422 UART, and PPS Input Glenair PN: 891-028-51SS-BRT1T-02								
Pin #	**Type**	**Signal Name**	**Pin #**	**Type**	**Signal Name**	**Pin #**	**Type**	**Signal Name**
1	PWR	GND	**18**	LVDS_IN	SPW1_DIN_P	**35**	PWR	GND
2	PWR	GND	**19**	LVDS_IN	SPW1_DIN_N	**36**	PWR	GND
3	LVDS_IN	SPW0_DIN_N	**20**	PWR	GND	**37**	ISO 11898	CANL_1
4	LVDS_IN	SPW0_DIN_P	**21**	LVDS_IN	SPW1_SIN_N	**38**	ISO 11898	CANH_1
5	PWR	GND	**22**	LVDS_IN	SPW1_SIN_P	**39**	PWR	GND
6	LVDS_OUT	SPW0_DOUT_P	**23**	PWR	GND	**40**	PWR	GND
7	LVDS_OUT	SPW0_DOUT_N	**24**	LVDS_OUT	SPW1_SOUT_P	**41**	RS422_OUT	422_0_TX_N
8	PWR	GND	**25**	LVDS_OUT	SPW1_SOUT_N	**42**	RS422_OUT	422_0_TX_P
9	LVDS_IN	SPW0_SIN_N	**26**	PWR	GND	**43**	RS422_IN	422_0_RX_N
10	LVDS_IN	SPW0_SIN_P	**27**	PWR	GND	**44**	RS422_IN	422_0_RX_P
11	PWR	GND	**28**	PWR	GND	**45**	PWR	GND
12	LVDS_OUT	SPW0_SOUT_P	**29**	RS422_IN	PPS_N	**46**	PWR	GND
13	LVDS_OUT	SPW0_SOUT_N	**30**	RS422_IN	PPS_P	**47**	RS422_IN	422_1_RX_N
14	PWR	GND	**31**	PWR	GND	**48**	RS422_IN	422_1_RX_P
15	LVDS_OUT	SPW1_DOUT_N	**32**	PWR	GND	**49**	RS422_OUT	422_1_TX_N
16	LVDS_OUT	SPW1_DOUT_P	**33**	ISO 11898	CANL_0	**50**	RS422_OUT	422_1_TX_P
17	PWR	GND	**34**	ISO 11898	CANH_0	**51**	PWR	GND

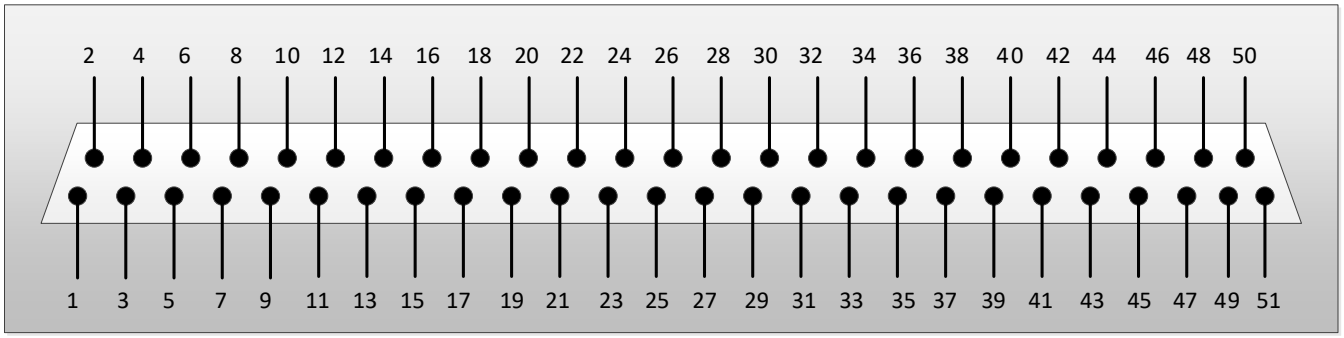


Figure 2. Glenair 51-pin Front Panel Receptacle Pinout

J1: 37-pin Front Panel Connector

Table 2. J1 Connector Pinlist

J1 – Connector Pinlist for Triple 10/100/1000Base-T Ethernet Ports Glenair PN: 891-028-37SS-BRT1T-02					
Pin #	**Type**	**Signal Name**	**Pin #**	**Type**	**Signal Name**
1	PAM-5	E0_A_P	**20**	PAM-5	E1_C_N
2	PAM-5	E0_A_N	**21**	PAM-5	E1_C_P
3	PWR	GND	**22**	PWR	GND
4	PAM-5	E0_B_N	**23**	PAM-5	E1_D_P
5	PAM-5	E0_B_P	**24**	PAM-5	E1_D_N
6	PWR	GND	**25**	PWR	GND
7	PAM-5	E0_C_P	**26**	PWR	GND
8	PAM-5	E0_C_N	**27**	PAM-5	E2_A_P
9	PWR	GND	**28**	PAM-5	E2_A_N
10	PAM-5	E0_D_N	**29**	PWR	GND
11	PAM-5	E0_D_P	**30**	PAM-5	E2_B_N
12	PWR	GND	**31**	PAM-5	E2_B_P
13	PWR	GND	**32**	PWR	GND
14	PAM-5	E1_A_N	**33**	PAM-5	E2_C_P
15	PAM-5	E1_A_P	**34**	PAM-5	E2_C_N
16	PWR	GND	**35**	PWR	GND
17	PAM-5	E1_B_P	**36**	PAM-5	E2_D_N
18	PAM-5	E1_B_N	**37**	PAM-5	E2_D_P
19	PWR	GND			

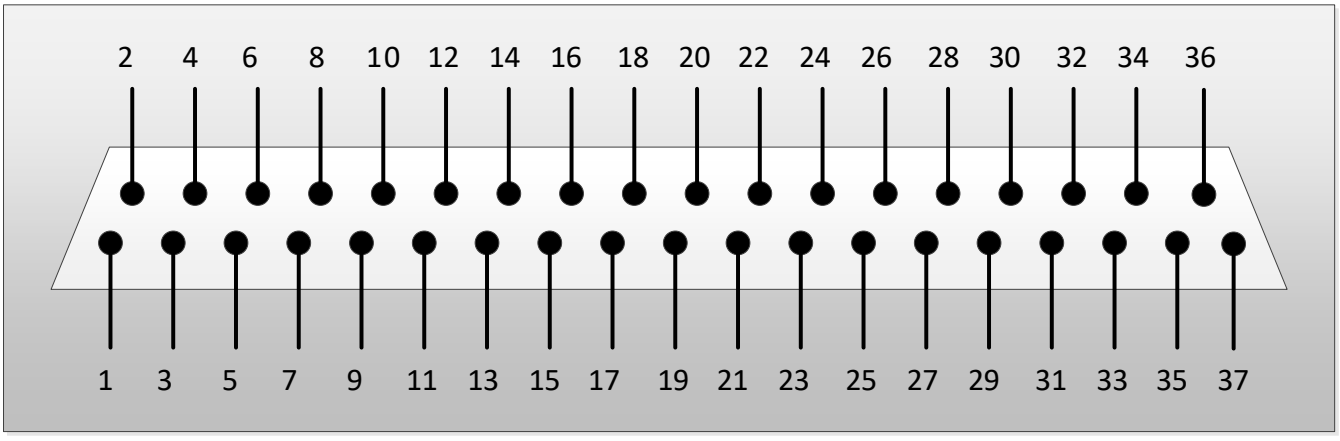


Figure 3. Glenair 37-pin Front Panel Receptacle Pinout

J15: Primary Mezzanine Connector

Table 3. J15 XMC+ Primary Connector Pinlist

J15 – XMC+ Primary Mezzanine Connector Pinlist Samtec PN: ASP-212954-01								
Pin Location	**Pin Name**	**Signal/Net Name**	**Pin Location**	**Pin Name**	**Signal/Net Name**	**Pin Location**	**Pin Name**	**Signal/Net Name**
A01	DP00+	SERDES_1_TX0_P	**C01**	3.3V	3.3V	**E01**	DP01-	SERDES_1_RX0_N
A02	GND	GND	**C02**	TRST#	TRST#	**E02**	GND	GND
A03	DP02+	SERDES_1_TX1_P	**C03**	3.3V	3.3V	**E03**	DP03-	SERDES_1_RX1_N
A04	GND	GND	**C04**	TCK	TCK	**E04**	GND	GND
A05	DP04+	SERDES_1_TX2_P	**C05**	3.3V	3.3V	**E05**	DP05-	SERDES_1_RX2_N
A06	GND	GND	**C06**	TMS	TMS	**E06**	GND	GND
A07	DP06+	SERDES_1_TX3_P	**C07**	3.3V	3.3V	**E07**	DP07-	SERDES_1_RX3_N
A08	GND	GND	**C08**	TDI	TDI	**E08**	GND	GND
A09	DP08+	FPGA_MEZ_CLK_P	**C09**	RPS	RPS	**E09**	DP09-	MEZ_SYNC_1_N
A10	GND	GND	**C10**	TDO	TDO	**E10**	GND	GND
A11	DP10+	MEZZ_PCIe_P	**C11**	MBIST#	MBIST#	**E11**	DP11-	MEZ_SYNC_2_N
A12	GND	GND	**C12**	GA1	GA1	**E12**	GND	GND
A13	DP12+	MEZZ_125_CLK_P	**C13**	3.3V AUX	3.3V AUX	**E13**	DP13-	MEZ_SYNC_3_N
A14	GND	GND	**C14**	GA2	GA2	**E14**	GND	GND
A15	DP14+	CNM1_LVDSIN_P	**C15**	RPS	TP2	**E15**	DP15-	MEZ_SYNC_4_N
A16	GND	GND	**C16**	MVMRO	MVMRO	**E16**	GND	GND
A17	DP16+	N/C	**C17**	RFU	RFU	**E17**	DP17-	N/C
A18	GND	GND	**C18**	RPS	RPS	**E18**	GND	GND
A19	DP18+	N/C	**C19**	RPS	RPS	**E19**	DP19-	N/C
B01	DP00-	SERDES_1_TX0_N	**D01**	DP01+	SERDES_1_RX0_P	**F01**	VPWR	VPWR
B02	GND	GND	**D02**	GND	GND	**F02**	MRSTI#	MRSTI#
B03	DP02-	SERDES_1_TX1_N	**D03**	DP03+	SERDES_1_RX1_P	**F03**	VPWR	VPWR
B04	GND	GND	**D04**	GND	GND	**F04**	MRSTO#	MRSTO#
B05	DP04-	SERDES_1_TX2_N	**D05**	DP05+	SERDES_1_RX2_P	**F05**	VPWR	+12V
B06	GND	GND	**D06**	GND	GND	**F06**	+12V	+12V
B07	DP06-	SERDES_1_TX3_N	**D07**	DP07+	SERDES_1_RX3_P	**F07**	VPWR	+12V
B08	GND	GND	**D08**	GND	GND	**F08**	-12V	-12V
B09	DP08-	FPGA_MEZ_CLK_N	**D09**	DP09+	MEZ_SYNC_1_P	**F09**	VPWR	+12V
B10	GND	GND	**D10**	GND	GND	**F10**	GA0	GA0
B11	DP10-	MEZZ_PCIe_N	**D11**	DP11+	MEZ_SYNC_2_P	**F11**	VPWR	+12V
B12	GND	GND	**D12**	GND	GND	**F12**	MPRESENT#	MPRESENT#
B13	DP12-	MEZZ_125_CLK_N	**D13**	DP13+	MEZ_SYNC_3_P	**F13**	VPWR	+12V
B14	GND	GND	**D14**	GND	GND	**F14**	MSDA	TMP_SDA
B15	DP14-	CNM1_LVDSIN_N	**D15**	DP15+	MEZ_SYNC_4_P	**F15**	VPWR	+12V
B16	GND	GND	**D16**	GND	GND	**F16**	MSCL	TMP_SCL
B17	DP16-	N/C	**D17**	DP17+	N/C	**F17**	RFU	RFU
B18	GND	GND	**D18**	GND	GND	**F18**	RPS	RPS
B19	DP18-	N/C	**D19**	DP19+	N/C	**F19**	RPS	RPS

Primary XMC Connector						
	A	B	C	D	E	F
1	SERDES_1_TX0_P	SERDES_1_TX0_N	3.3V	SERDES_1_RX0_P	SERDES_1_RX0_N	VPWR
2	GND	GND	TRST#	GND	GND	MRSTI#
3	SERDES_1_TX1_P	SERDES_1_TX1_N	3.3V	SERDES_1_RX1_P	SERDES_1_RX1_N	VPWR
4	GND	GND	TCK	GND	GND	MRSTO#
5	SERDES_1_TX2_P	SERDES_1_TX2_N	3.3V	SERDES_1_RX2_P	SERDES_1_RX2_N	+12V
6	GND	GND	TMS	GND	GND	+12V
7	SERDES_1_TX3_P	SERDES_1_TX3_N	3.3V	SERDES_1_RX3_P	SERDES_1_RX3_N	+12V
8	GND	GND	TDI	GND	GND	-12V
9	FPGA_MEZ_CLK_P	FPGA_MEZ_CLK_N	RPS	MEZ_SYNC_1_P	MEZ_SYNC_1_N	+12V
10	GND	GND	TDO	GND	GND	GA0
11	MEZZ_PCIe_P	MEZZ_PCIe_N	MBIST#	MEZ_SYNC_2_P	MEZ_SYNC_2_N	+12V
12	GND	GND	GA1	GND	GND	MPRESENT#
13	MEZZ_125_CLK_P	MEZZ_125_CLK_N	3.3V AUX	MEZ_SYNC_3_P	MEZ_SYNC_3_N	+12V
14	GND	GND	GA2	GND	GND	TMP_SDA
15	CNM1_LVDSIN_P	CNM1_LVDSIN_N	RPS	MEZ_SYNC_4_P	MEZ_SYNC_4_N	+12V
16	GND	GND	MVMRO	GND	GND	TMP_SCL
17	N/C	N/C	RFU	N/C	N/C	RFU
18	GND	GND	RPS	GND	GND	RPS
19	N/C	N/C	RPS	N/C	N/C	RPS

Figure 4. J15 XMC+ Primary Connector Pinout

J16: Secondary Mezzanine Connector

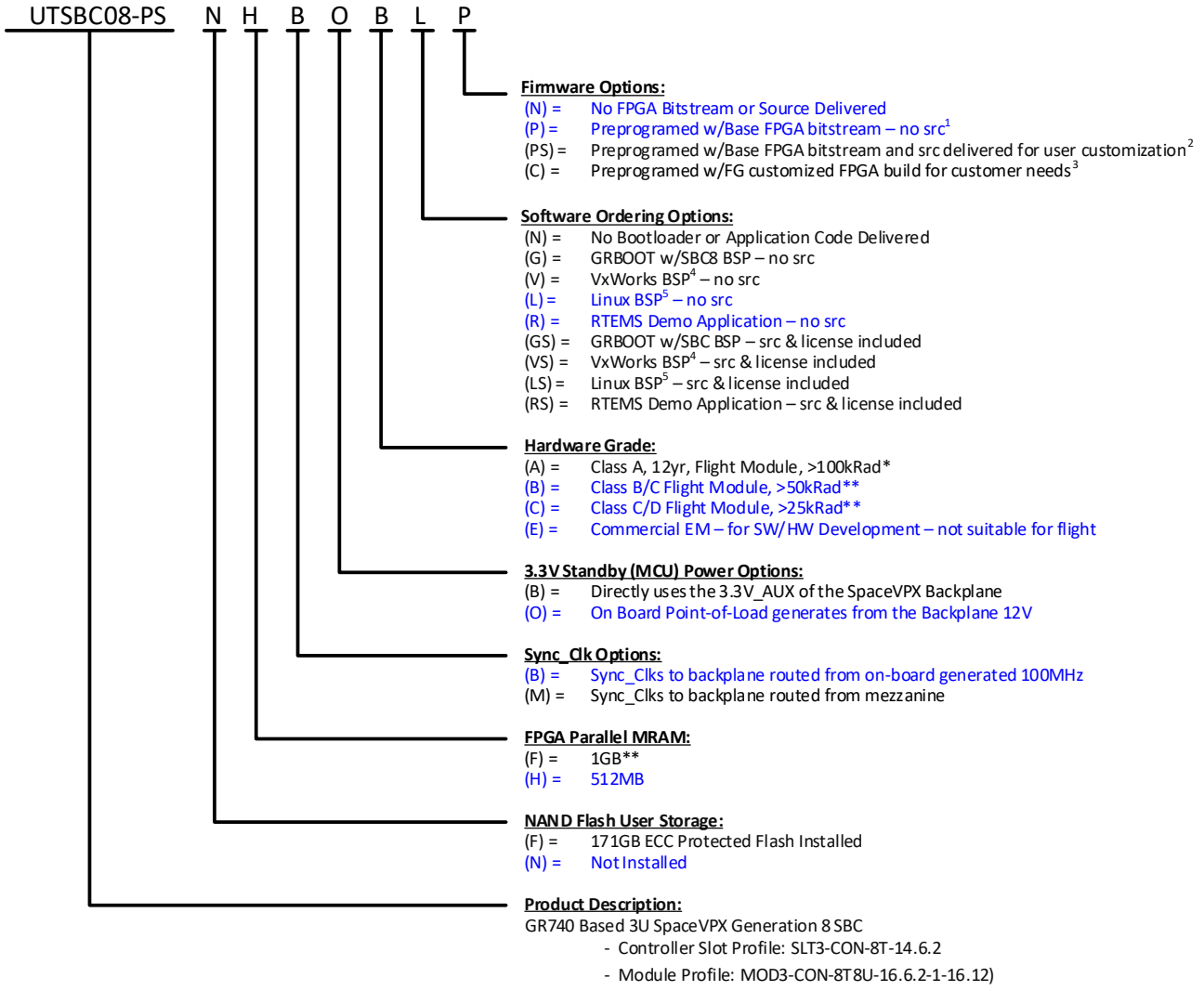
Table 4. J16 XMC+ Secondary Connector Pinlist

J16 – XMC+ Secondary Mezzanine Connector Pinlist Samtec PN: ASP-212954-01								
Pin Location	**Pin Name**	**Signal/Net Name**	**Pin Location**	**Pin Name**	**Signal/Net Name**	**Pin Location**	**Pin Name**	**Signal/Net Name**
A01	DP00+	MEZZ_50MHZ_CLK	**C01**	UD	PCI_AD0	**E01**	DP01-	N/C
A02	GND	GND	**C02**	UD	PCI_AD1	**E02**	GND	GND
A03	DP02+	N/C	**C03**	UD	PCI_AD2	**E03**	DP03-	N/C
A04	GND	GND	**C04**	UD	PCI_AD3	**E04**	GND	GND
A05	DP04+	N/C	**C05**	UD	PCI_AD4	**E05**	DP05-	FPGA_PCI_GNT
A06	GND	GND	**C06**	UD	PCI_AD5	**E06**	GND	GND
A07	DP06+	GR740_PCI_REQ0	**C07**	UD	PCI_AD6	**E07**	DP07-	PPS_TO_FROM_MEZ
A08	GND	GND	**C08**	UD	PCI_AD7	**E08**	GND	GND
A09	DP08+	PCI_INTD	**C09**	UD	PCI_AD8	**E09**	DP09-	FPGA_MEZ_8
A10	GND	GND	**C10**	UD	PCI_AD9	**E10**	GND	GND
A11	DP10+	FPGA_MEZ_7	**C11**	UD	PCI_AD10	**E11**	DP11-	FPGA_MEZ_4
A12	GND	GND	**C12**	UD	PCI_AD11	**E12**	GND	GND
A13	DP12+	FPGA_MEZ_2	**C13**	UD	PCI_AD12	**E13**	DP13-	GR740_PCI_REQ1
A14	GND	GND	**C14**	UD	PCI_AD13	**E14**	GND	GND
A15	DP14+	PCI_STOP	**C15**	UD	PCI_AD14	**E15**	DP15-	PCI_IDSEL
A16	GND	GND	**C16**	UD	PCI_AD15	**E16**	GND	GND
A17	DP16+	PCI_PAR	**C17**	UD	PCI_AD16	**E17**	DP17-	PCI_SERR
A18	GND	GND	**C18**	UD	PCI_AD17	**E18**	GND	GND
A19	DP18+	PCI_TRDY	**C19**	UD	PCI_AD18	**E19**	DP19-	PCI_HOSTN
B01	DP00-	N/C	**D01**	DP01+	GR740_GPIO2_2	**F01**	UD	MEZZ_PCI_CLK
B02	GND	GND	**D02**	GND	GND	**F02**	UD	PCI_FRAME
B03	DP02-	N/C	**D03**	DP03+	N/C	**F03**	UD	PCI_AD19
B04	GND	GND	**D04**	GND	GND	**F04**	UD	PCI_AD20
B05	DP04-	N/C	**D05**	DP05+	N/C	**F05**	UD	PCI_AD21
B06	GND	GND	**D06**	GND	GND	**F06**	UD	PCI_AD22
B07	DP06-	FPGA_PCI_REQ	**D07**	DP07+	GR740_PCI_GNT0	**F07**	UD	PCI_AD23
B08	GND	GND	**D08**	GND	GND	**F08**	UD	PCI_AD24
B09	DP08-	PCI_INTA	**D09**	DP09+	PCI_INTC	**F09**	UD	PCI_AD25
B10	GND	GND	**D10**	GND	GND	**F10**	UD	PCI_AD26
B11	DP10-	FPGA_MEZ_5	**D11**	DP11+	FPGA_MEZ_6	**F11**	UD	PCI_AD27
B12	GND	GND	**D12**	GND	GND	**F12**	UD	PCI_AD28
B13	DP12-	FPGA_MEZ_1	**D13**	DP13+	FPGA_MEZ_3	**F13**	UD	PCI_AD29
B14	GND	GND	**D14**	GND	GND	**F14**	UD	PCI_AD30
B15	DP14-	PCI_INTB	**D15**	DP15+	GR740_PCI_GNT1	**F15**	UD	PCI_AD31
B16	GND	GND	**D16**	GND	GND	**F16**	UD	PCI_CBE0
B17	DP16-	PCI_PERR	**D17**	DP17+	PCI_DEVSEL	**F17**	UD	PCI_CBE1
B18	GND	GND	**D18**	GND	GND	**F18**	UD	PCI_CBE2
B19	DP18-	PCI_M66EN	**D19**	DP19+	PCI_IRDY	**F19**	UD	PCI_CBE3

Secondary XMC Connector						
	A	B	C	D	E	F
1	MEZZ_50MHZ_CLK	N/C	PCI_AD0	GR740_GPIO2_2	N/C	MEZZ_PCI_CLK
2	GND	GND	PCI_AD1	GND	GND	PCI_FRAME
3	N/C	N/C	PCI_AD2	N/C	N/C	PCI_AD19
4	GND	GND	PCI_AD3	GND	GND	PCI_AD20
5	N/C	N/C	PCI_AD4	N/C	FPGA_PCI_GNT	PCI_AD21
6	GND	GND	PCI_AD5	GND	GND	PCI_AD22
7	GR740_PCI_REQ0	FPGA_PCI_REQ	PCI_AD6	GR740_PCI_GNT0	PPS_TO_FROM_MEZ	PCI_AD23
8	GND	GND	PCI_AD7	GND	GND	PCI_AD24
9	PCI_INTD	PCI_INTA	PCI_AD8	PCI_INTC	FPGA_MEZ_8	PCI_AD25
10	GND	GND	PCI_AD9	GND	GND	PCI_AD26
11	FPGA_MEZ_7	FPGA_MEZ_5	PCI_AD10	FPGA_MEZ_6	FPGA_MEZ_4	PCI_AD27
12	GND	GND	PCI_AD11	GND	GND	PCI_AD28
13	FPGA_MEZ_2	FPGA_MEZ_1	PCI_AD12	FPGA_MEZ_3	GR740_PCI_REQ1	PCI_AD29
14	GND	GND	PCI_AD13	GND	GND	PCI_AD30
15	PCI_STOP	PCI_INTB	PCI_AD14	GR740_PCI_GNT1	PCI_IDSEL	PCI_AD31
16	GND	GND	PCI_AD15	GND	GND	PCI_CBE0
17	PCI_PAR	PCI_PERR	PCI_AD16	PCI_DEVSEL	PCI_SERR	PCI_CBE1
18	GND	GND	PCI_AD17	GND	GND	PCI_CBE2
19	PCI_TRDY	PCI_M66EN	PCI_AD18	PCI_IRDY	PCI_HOSTN	PCI_CBE3

Figure 5. J16 XMC+ Secondary Connector Pinout

Preliminary Ordering Information (Not yet approved part numbering)



Note: Ordering options highlighted in *BLUE* text represent standard ordering configurations. The remaining options require an RFP to coordinate pricing adjustments to accommodate necessary build modifications, BoM implications, and potential licensing requirements.

*** Not currently a standard offering, but a custom version based on SBC8 can be created if needed by your project. Please contact factory to discuss.**

**** These grades of product are based on completion of flight qualification expected to complete 4Q2025**

1. Base FPGA Bitstream is designed to allow GR740 access to all ports, memories, etc. See the following section for a list of IPs & interfaces available in the standard firmware build.
2. Allows user to make changes to the FPGA code. However, this option will require a separately purchased licensing for the GRLIB IP used. If the GRLIP IP is not desired, it is recommended to procure the SBC08 hardware with the "N" – No FPGA bitstream or source delivered.
3. Frontgrade will bid the NRE and per board royalty cost of custom FPGA code in a separate quote in response to a RFP
4. User needs to purchase a separate source license from WindRiver for VxWorks. The SW delivery includes the architectural port (BSP) for VxWorks
5. Linux Distribution not included

Table 5. SBC8 FPGA GR LIB IP Build Options

Standard Build Firmware	GRLIB IP Core	GRIP Section
Yes	GRSPW2	§70
Yes	GRETH_GBIT	§49
Yes	GRGPIO	§56
No	GRHSSL	§58
Yes	SPIMASTER/POSLAVE	§120/§121
No	NANDFCTRL2	§105
Yes	FTMCTRL	§31
Yes	GRPCI2	§61
Yes	I2CMST	§86

Revision History

Date	Revision #	Author	Change Description	Page #
12/13/24	1.0	TLM	Initial DRAFT	All

Datasheet Definitions

	Definition
Advanced Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet or Product Brief	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet or Product Brief	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.