AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL

CAES

PRODUCT INFORMATION NOTICE

1. TITLE	2. DOCUMENT NUMBER
MICROCIRCUIT, MEMORY,DIGITAL,CMOS, 512 X 8-BIT, RADIATION-HARDENED SRAM MONOLITHIC SILICON	SPO-2018-PIN-0001
	3. DATE *(Year, Month, Date)* 2018, Oct, 1
4. MANUFACTURER NAME AND ADDRESS CAES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486	5. MANUFACTURER POINT OF CONTACT NAME Peter Nelson
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8. CAGE CODE	9. BLANK	10. PRODUCT IDENTIFICATION CODE	11. BASE PART
65342		See Below	See Below
12. BLANK		13. SMD NUMBER See Below	14. DEVICE TYPE DESIGNATOR See Below
		15. RHA LEVELS D, P, L	16. QML LEVEL Q, V
		17. NON QML LEVEL N/A	18. GIDEP NUMBER **GB4-I-19-0002**

19. DESCRIPTION (FOR NEW PRODUCTS, PROVIDE AVAILABILITY DATE AND LEAD TIME)

Summary: This ADEPT adds two guaranteed by design AC timing specifications to both the datasheet and SMD (t_{AVSK} and t_{AVET2}) which where recommendations of the previously documented application note (AN-MEM-002). Datasheet changes are also noted herein. This change replaces the data from the app note in the datasheet and adds data to the SMD to ensure that the user does not miss the timing info.

SMD 99607 drawing bulletin table was updated to align the part availability with the data in the DLA Standard Microcircuit Cross-Reference.

Also, the extended industrial temperature option is being removed, leaving only MIL temp range parts that can be ordered. Last buy date for these parts is May 10th, 2019.

Product Name:	Manufacturer Part Number	SMD #	Device Type
4M Asynchronous SRAM	UT8Q512E	5962-99607	05
4M Asynchronous SRAM	UT9Q512E	5962-00536	05

NOTE: THIS DOCUMENT IS PUBLISHED FOR INFORMATION PURPOSES AND MAY PROVIDE FORWARD LOOKING STATEMENTS THAT ARE SUBJECT TO CHANGE. THE USERS SHOULD CONTACT THEIR LOCAL CAES SALES OFFICE FOR ANY ACTIONABLE CONTENT DESCRIBED HEREIN.

20. ADEPT REPRESENTATIVE	21. SIGNATURE	22. DATE
Tim Meade		**10/01/18**

Section 1: SMD changes

TABLE 1A Electrical performance characteristics.

Add parameters t_{AVSK} and t_{AVET2}

Test	Symbol	Test conditions -55°C < T_C < +125°C (Devices 01,03,05) -40°C < T_C < +125°C (Devices 02,04,06) +4.5 V < V_{DD} < +5.5 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Functional test		See 4.4.1c, V_{IH} = V_{DD} -0.5V	7,8A,8B	All		1/	
Address valid to address valid skew time XX/	t_{AVSK}	See figures 4 and 5.	9,10,11	See above table		4	ns
		M,D,P,L	9	All	1/		
Address setup time for read (E – controlled) XX/	t_{AVET2}		9,10,11	See above table	-4		ns
		M,D,P,L	9	All		1/	

Add note 12 designation to t_{AVAV} parameter

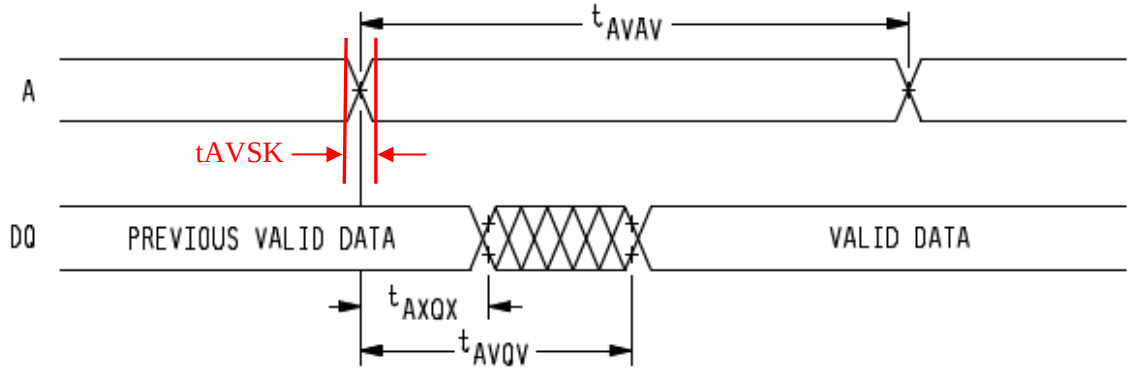
Read cycle time 6/, YY/	t_{AVAV}	See figures 4 and 5.	9,10,11	01,02	25		ns
				03,04, 05, 06	20		
		M,D,P,L	9	All	1/		

Add two notes to Table 1A

XX/ Guaranteed by design
YY/ Address changes prior to satisfying t_{AVAV} minimum is an invalid operation

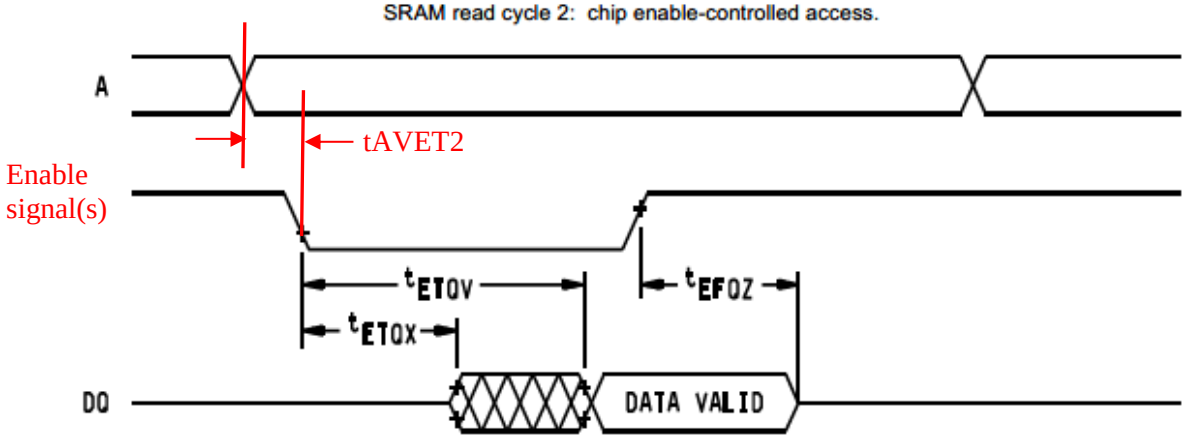
Add timing parameters to SRAM read cycle 1 and read cycle 2

SRAM read cycle 1: address access.



Note: $\overline{E}$ and $\overline{G} \leq V_{IL}$(max) and $\overline{W} \geq V_{IH}$ (min).

SRAM read cycle 2: chip enable-controlled access.



Note: $\overline{G} \leq V_{IL}$(max) and $\overline{W} \geq V_{IH}$ (min).

FIGURE 5. Timing waveforms - Continued.

Section 2: Datasheet changes

Datasheet
Add last sentences to the end of both paragraphs

READ CYCLE

A combination of $\overline{W}$ greater than V_{IH} (min) and $\overline{E}$ less than V_{IL} (max) defines a read cycle. Read access time is measured from the latter of Chip Enable, Output Enable, or valid address to valid data output. Read cycles initiate with the assertion of chip enable or any address input change while chip enable is asserted.

SRAM Read Cycle 1, the Address Access in figure 4a is initiated by a change in address inputs while the chip is enabled with $\overline{G}$ asserted and $\overline{W}$ deasserted. Valid data appears on data outputs DQ(7:0) after the specified t_{AVQV} is satisfied. Outputs remain active throughout the entire cycle. As long as chip enable and output enable are active, the address inputs may change at a rate equal to the minimum read cycle time (t_{AVAV}). Changing addresses prior to satisfying tAVAV minimum results in an invalid operation. Invalid read cycles will require re-initialization.

The single die devices will say “read cycles initiate with assertion of chip enable and address changes while chip enable is asserted”. The MCM parts with multiple chip enables will say “read cycle initiates with the assertion of any chip enable and also address changes while any chip enable is asserted”.

AC Characteristics read cycle table
Adding parameters t_{AVSK} and t_{AVET2} and two additional notes

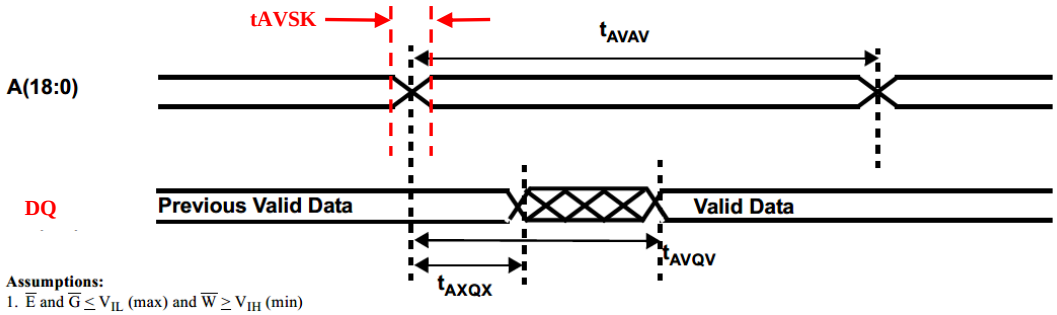
AC CHARACTERISTICS READ CYCLE (Pre/Post-Radiation)*

-55°C to +125°C for (C) screening and -40°C to +125°C for (W) screening (V_{DD} = 5.0V + 10%)

SYMBOL	PARAMETER	MIN	MAX	UNIT
tAVAV[1,6]	Read cycle time	20		ns
tAVSK[5]	Adress valid to address valid skew time		4	ns
tAVQV	Read access time		20	ns
tAXQX	Output hold time	3		ns
tGLQX	$\overline{G}$-controlled Output Enable time	0		ns
tGLQV	$\overline{G}$-controlled Output Enable time (Read Cycle 3)		10	ns
tGHQZ[2]	$\overline{G}$-controlled output three-state time		10	ns
tETQX[3]	$\overline{E}$-controlled Output Enable time	3		ns
tAVET2[5]	Address setup time for read ($\overline{E}$-controlled)	-4		ns
tETQV[3]	$\overline{E}$-controlled access time		20	ns
tEFQZ[1,2,4]	$\overline{E}$-controlled output three-state time		10	ns

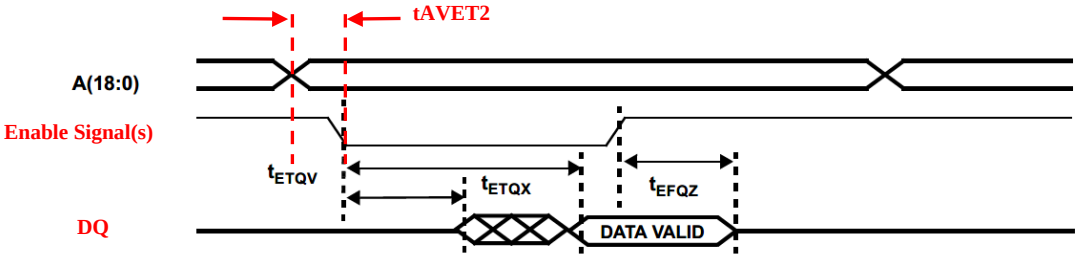
Notes: * Post-radiation performance guaranteed at 25°C per MIL-STD-883 Method 1019.
1. Functional test.
2. Three-state is defined as a 500mV change from steady-state output voltage.
3. The ET (chip enable true) notation refers to the falling edge of En. SEU immunity does not affect the read parameters.
4. The EF (chip enable false) notation refers to the rising edge of En. SEU immunity does not affect the read parameters.
5. Guaranteed by design.
6. Address changes prior to satisfying tAVAV minimum is an invalid operation.

SRAM Read cycle 1 and 2
Adding parameters tAVSK and tAVET2 to timing diagrams



Assumptions:
1. $\overline{E}$ and $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 4a. SRAM Read Cycle 1: Address Access



Assumptions:
1. $\overline{G} \leq V_{IL}$ (max) and $\overline{W} \geq V_{IH}$ (min)

Figure 4b. SRAM Read Cycle 2: Chip Enable-Controlled Access

Ordering Information:

- Remove device type 06 from SMD PN callout
- Remove (W) screening from UT PN callout