AEROSPACE DATA EXCHANGE PROGRAM TRANSMITTAL

PRODUCT CHANGE NOTICE

CAES

1. TITLE	2. DOCUMENT NUMBER
MICROCIRCUIT, DIGITAL, CMOS, RADIATION HARDENED, 32-BIT FAULT-TOLERANT V8/LEON 3FT PROCESSOR, MONOLITHIC SILICON	**SPO-2013-PCN-0003**
	3. DATE *(Year, Month, Date)* **2013, February, 27**
4. MANUFACTURER NAME AND ADDRESS CAES 4350 CENTENNIAL BOULEVARD COLORADO SPRINGS, COLORADO 80907-3486	5. MANUFACTURER POINT OF CONTACT NAME **James Nagy**
	6. MANUFACTURER POINT OF CONTACT TELEPHONE **719-594-8417**
	7. MANUFACTURER POINT OF CONTACT EMAIL **james.nagy@cobhamaes.com**

8. CAGE CODE	9. EFFECTIVE DATE	10. PRODUCT IDENTIFICATION CODE	11. BASE PART
65342	**May 28, 2009**	**WG07A**	**UT699**
12. BLANK		13. SMD NUMBER **5962-08228**	14. DEVICE TYPE DESIGNATOR **01, 02**
		15. RHA LEVELS **R, F**	16. QML LEVEL **Q, V**
		17. NON QML LEVEL **E, P**	18. BLANK

19. PRODUCT CHANGE

In reference to the corrective action listed in GIDEP GB4-P-13-02 and CAES ADEPT SPO-2013-PA-0002, CAES is working in coordination with DLA Land and Maritime to institute the following changes to the SMD reference in block 13 of this transmittal.

The changes described in this transmittal reflect the essence of the changes that will occur in the SMD. They do not dictate the precise form in which the SMD will represent the information.

Table IA (sheet 6)

ADDED:

For I_{DDCS} add RHA level 'F' SUBGROUP '1' with Max Limit of 20mA.

Note: The UT699 has always been tested to this limit. CAES inadvertently omitted the test limit in the initial SMD.

Table IA (sheet 12)

PREVIOUS:

Test	Symbol	Min	Max	Unit
PCI_RST active time after power stable	t_{22} 10/	1	--	ms
PCI_RST active time after PCI_CLK stable	t_{23} 10/	100	--	us
PCI_RST active to output float delay	t_{24} 10/		40	ns

CONTINUED ON NEXT SHEET

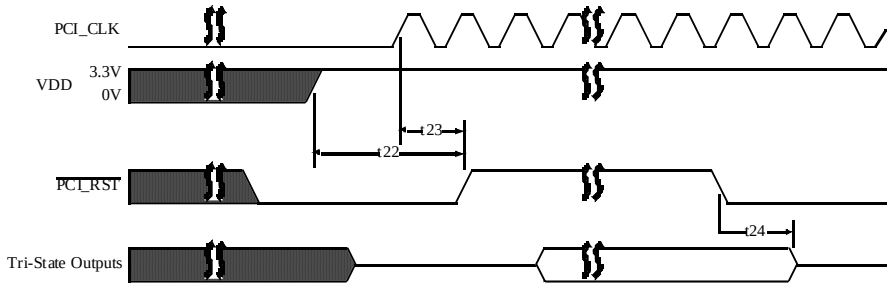
19. PRODUCT CHANGE CONTINUED

CORRECTED:

Test	Symbol	Min	Max	Unit
PCI_CLK ↑ to RESET deassertion	t_{22} 10/	10	--	PCI clocks
PCI_CLK ↑ to PCI_RST deassertion	t_{23a} 10/	10	--	PCI clocks
PCI_RST assertion to PCI_CLK idle	t_{23b} 10/	10	--	PCI clocks
PCI_RST assertion to output high-Z (PCI_AD[31:0], PCI_C/BE[3:0], PCI_PAR, PCI_FRAME, PCI_IRDY, PCI_TDRY, PCI_STOP, and PCI_DEVSEL)	t_{24} 10/	--	40	ns

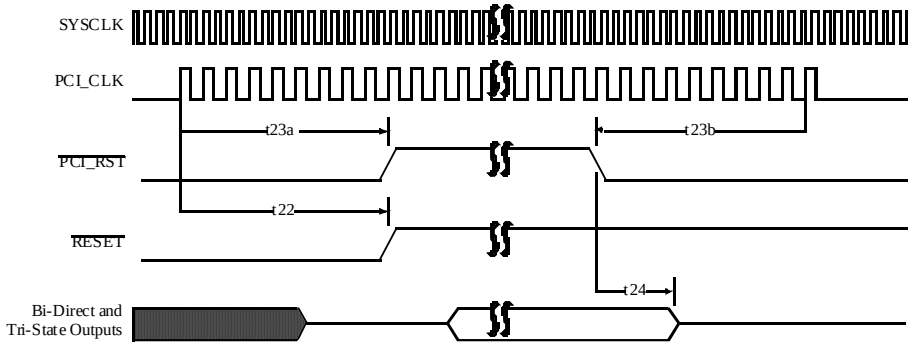
Figure 13 (sheet 30)

PREVIOUS:



PCI RESET TIMING DIAGRAM

CORRECTED:



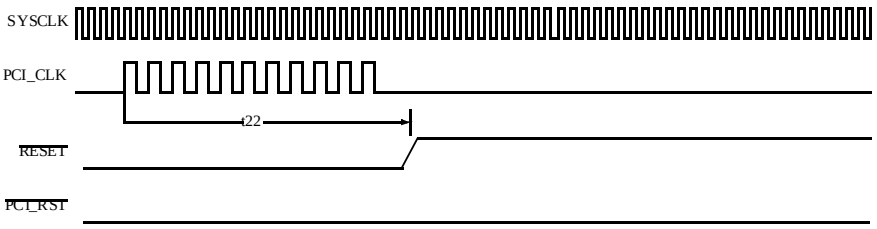
SYSTEM AND PCI RESET TIMING DIAGRAM

CONTINUED ON NEXT SHEET

19. PRODUCT CHANGE CONTINUED

Figure 14 (sheet 30)

ADDED:



SYSTEM RESET TIMING WHEN PCI IS NOT USED

20. DISPOSITIONARY RECOMMENDATION:	CHECK & USE AS IS ☐	CONTACT MANUFACTURER ☐	REMOVE & REPLACE ☐	CORRECT & USE AS SPECIFIED ☐
21. ADEPT REPRESENTATIVE **Timothy L. Meade**	22. SIGNATURE Timothy L Meade			23. DATE **27 February, 2013**