FRONTGRADE

APPLICATION NOTE

UT65CML8X8FD XPS

Frontgrade UT65CML8X8FD XPS +Xilinx XQRKU060 FPGA SERDES Interoperability Demonstration

9/11/2023

Frontgrade UT65CML8X8FD Crosspoint Switch (XPS) + Xilinx XQRKU060 FPGA SERDES - Interoperability Demonstration

This Application Note (AN) serves to document the successful interfacing and interoperability demonstration of the Frontgrade UT65CML8X8FD Crosspoint Switch (XPS) with the Xilinx XQRKU060 FPGA SERDES.

The Xilinx Vivado IBERT module was used to run and monitor a data loop-back test through the UT65CML8X8FD-EVB and the Xilinx XQRKU060 FPGA SERDES. Measured results show good data eye opening and low bit error rate (BER) at the specified 3.125 Gbps data rate using a 2^7-1 PRBS data pattern.

Test Equipment – List and Setup

Test Equipment – List

Agilent N4903B J-BERT Pat. Gen./ BER Checker 12.5 Gbps (XPS Eval. Board. Check-Out)

Keysight MSOS604A 6 GHz, 4-Ch. O'Scope (XPS Eval. Board. Check-Out)

Agilent/Keysight E3648A Dual Output DC Power Supply

Alpha Data XQRKU060 FPGA Reference Design Board: ADA-SDEV-KIT3/C

- Alpha Data Configuration Daughter Card: ADA-SDEV-CFG1 (USB-to-JTAG)
- Terasic XTS-FMC FMC-to-SMA Daughter Card; FMC Conn. Pin D32 Removed: 3P3VAUX-3P3V Short!
- Corsair CX650 Computer Power Supply

PC Laptop #1: Xilinx Vivado FPGA Configuration SW – IBERT Example Module

National Instruments (NI) Digilent JTAG-HS3 Programming Cable (USB-to-JTAG)

Frontgrade UT65CML8X8FD-EVB XPS Eval. Board: S/N 003, WQ04A IC, C-BGA Pkg., Soldered DUT

PC Laptop #2: UT65CML8X8FD-EVB SW GUI

National Instruments (NI) USB-6501 USB-to-SPI Port Interface Adapter (Pod)

18 GHz SMA F-F Cables, VDC Banana Jack Cables

Test Equipment – Setup

Setup – XPS + XQRKU060 Loop-Back Test Bench

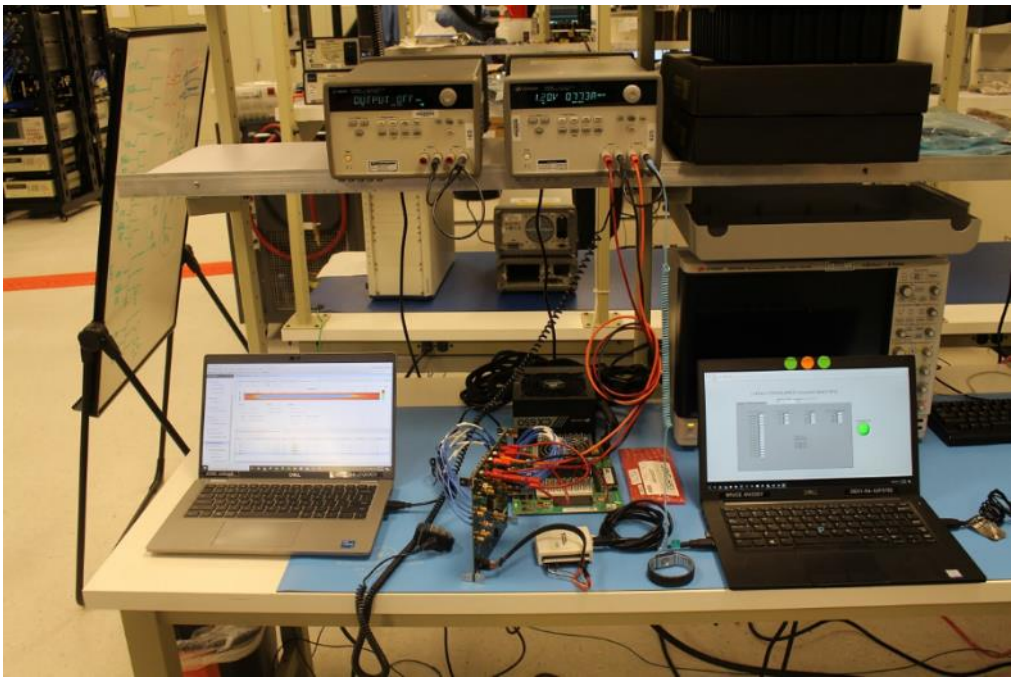

Figure 1: Test Setup – XPS + XQRKU060 Loop-Back Test Bench

Setup – XPS+XQRKU060 Loop-Back Test: XPS EVB

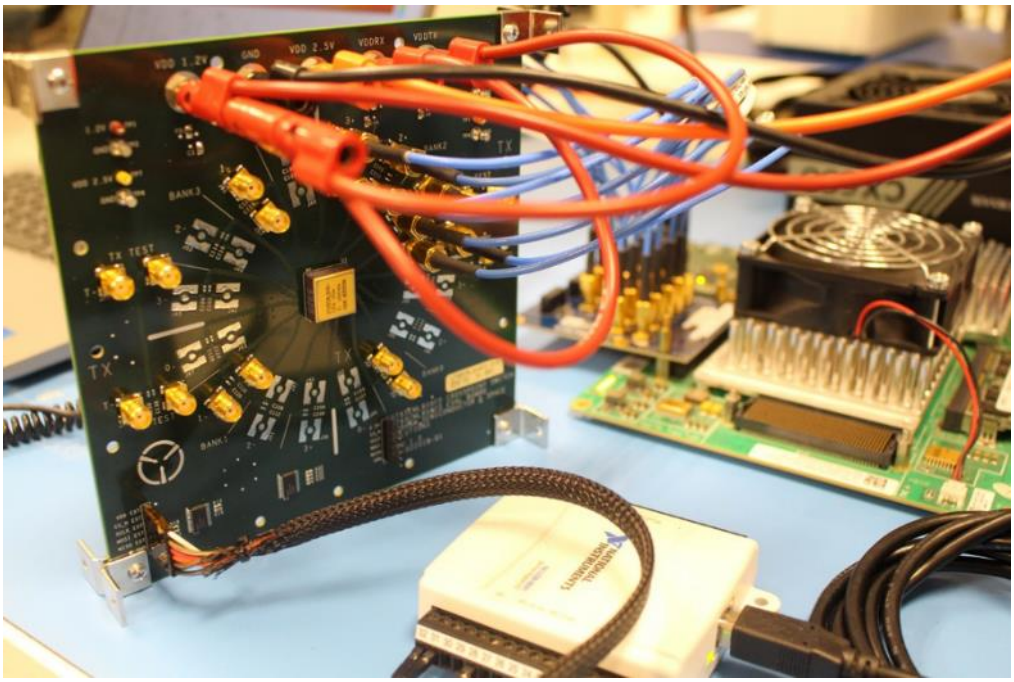

Figure 2: Test Setup – XPS+XQRKU060 Loop-Back Test: XPS EVB

Setup – XPS+XQRKU060 Loop-Back Test: XPS EVB

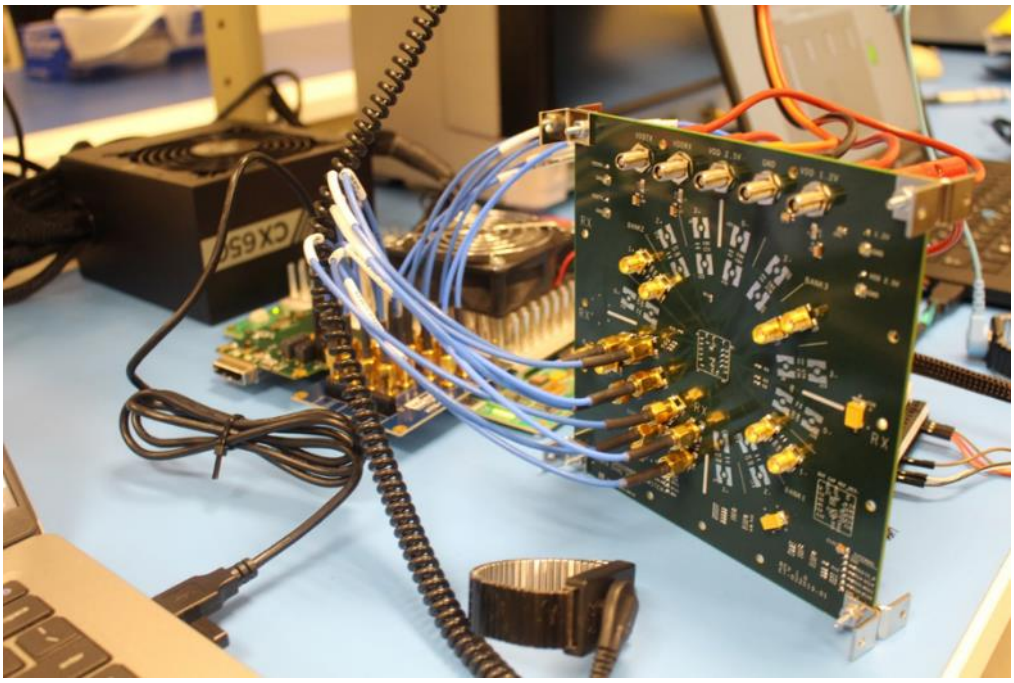

Figure 3: Test Setup – XPS+XQRKU060 Loop-Back Test: XPS EVB

Setup – Alpha Data XQRKU060 FPGA Reference Design Board

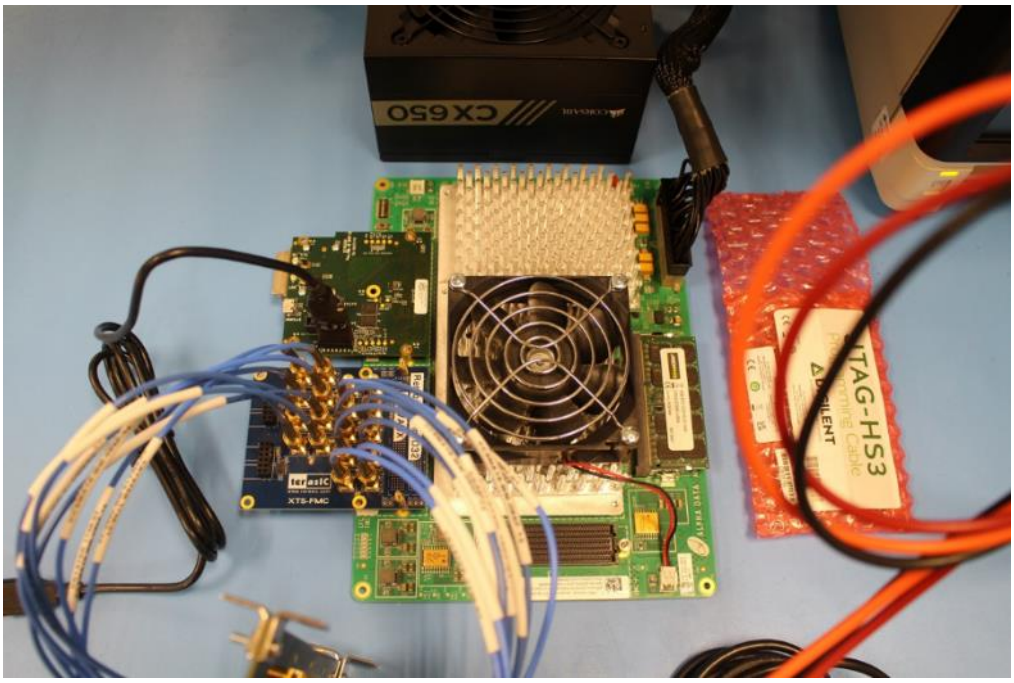

Figure 4: Test Setup – Alpha Data XQRKU060 FPGA Reference Design Board

Setup – Terasic XTS-FMC Daughter Card

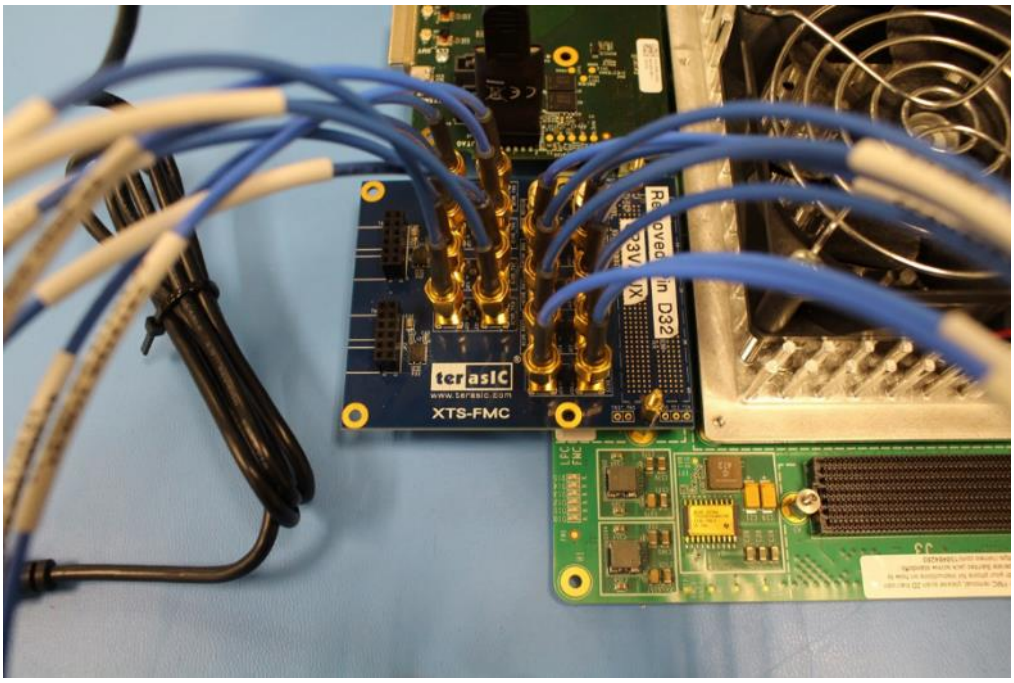

Figure 5: Test Setup – Terasic XTS-FMC Daughter Card

Setup – XQRKU060 SERDES Only Loop-Back Test Bench

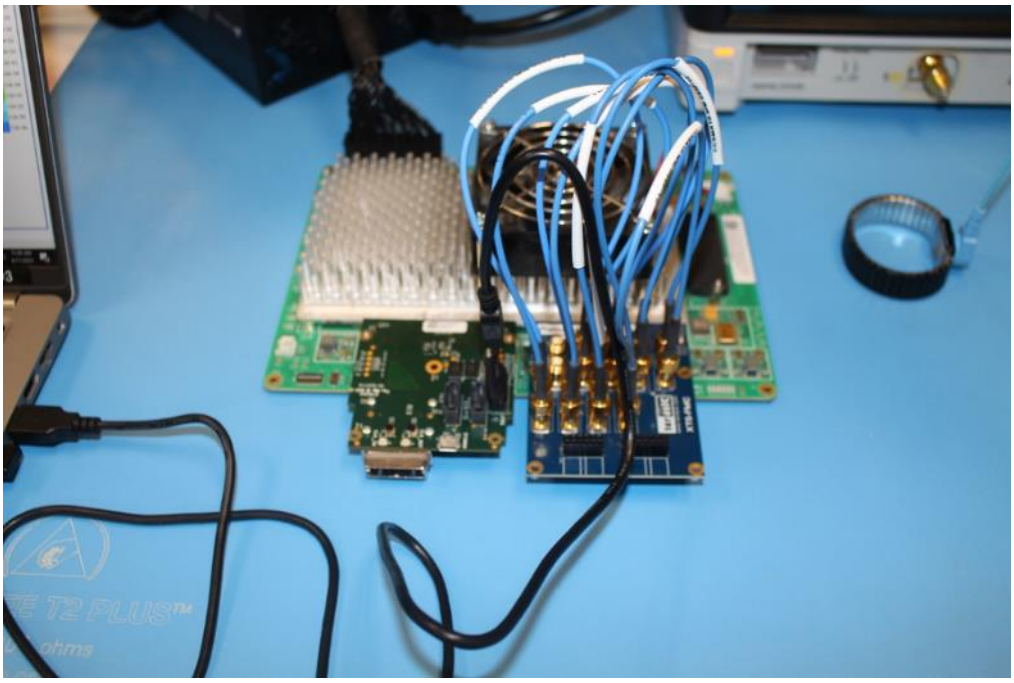

Figure 6: Test Setup – XQRKU060 SERDES Only Loop-Back Test Bench

Setup – XPS EVB RX EQ Channel Optimization Test Bench

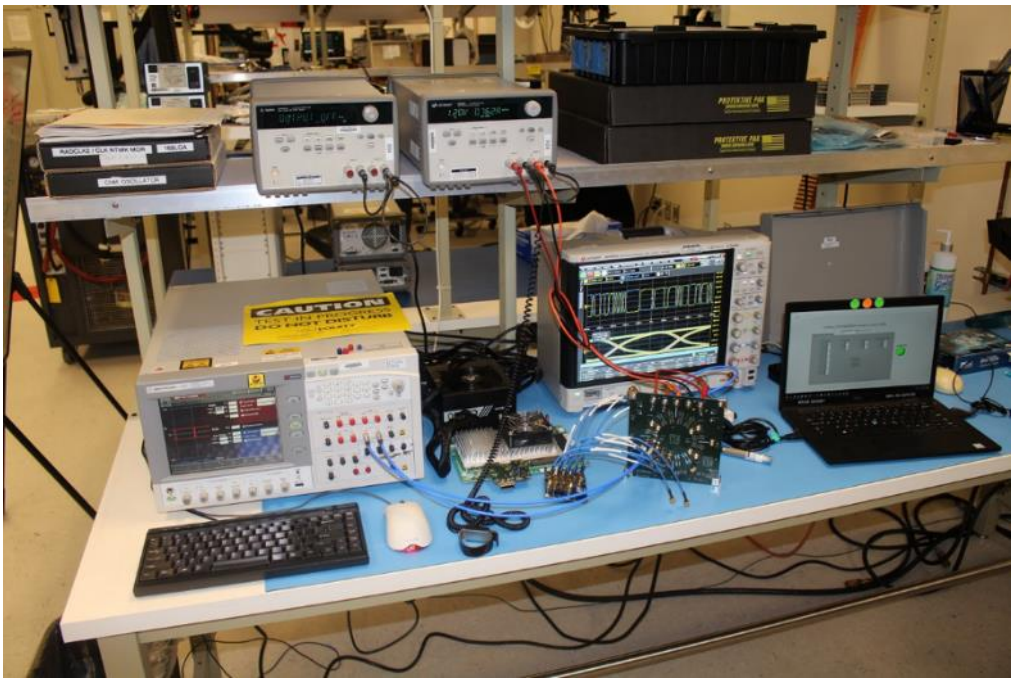

Figure 7: Test Setup – UT65CML8X8FD-EVB XPS EVB RX EQ Channel Optimization Test Bench

Settings

XPS + XQRKU060 SERDES Interop. Demo.

Vivado v. 2022.2 IBERT Loop-Back Test

UT65CML8X8FD-EVB Eval. Board Signal Path: XPS RX Bank 0[3:0] → TX Bank 2[3:0]

UT65CML8X8FD-EVB Eval. Board RX EQ: XPS Only Optimization

RX EQ Setting = 0x17

Xilinx XQRKU060 FPGA MGT SERDES Quad 225[3:0]

3.125 Gbps Data Rate: XAUI/10GbE; PRBS 27-1 Data Pattern - Approximates 8b-10b Encoded/Balanced Data, XPS RX EQ = 0x17

Vivado IBERT IL = 4dB (Default = 20dB); Amplitude = 390mVp-p, diff.; XPS VDDx=1.20V (All VDD ex. VDD_25), VDD_25=2.50V

Measured Results

Vivado IBERT Data Eye: XQRKU060 SERDES Quad 225 + XPS: Ch. 3

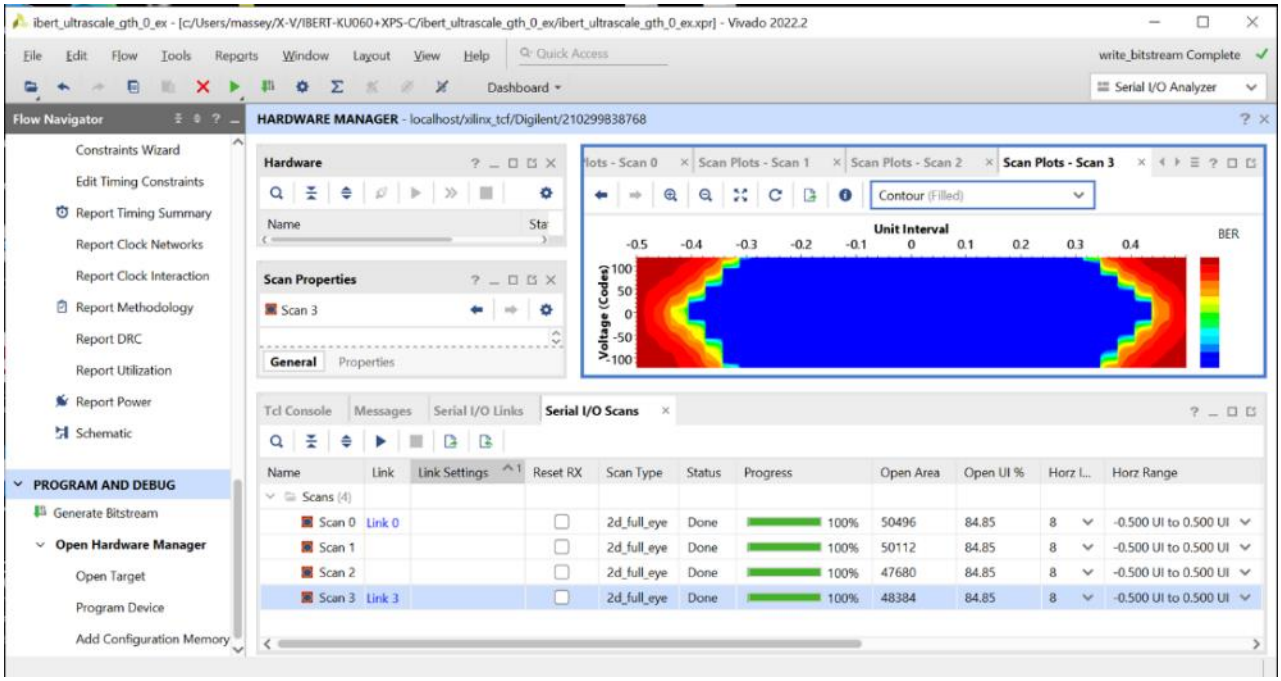

Figure 8: Xilinx Vivado IBERT Data Eye: XQRKU060 SERDES Quad 225 + UT65CML8X8FD XPS, Ch. 3 – Eye Opening: UI %

Vivado IBERT Data Eye: XQRKU060 SERDES Quad 225 + XPS: Ch. 3

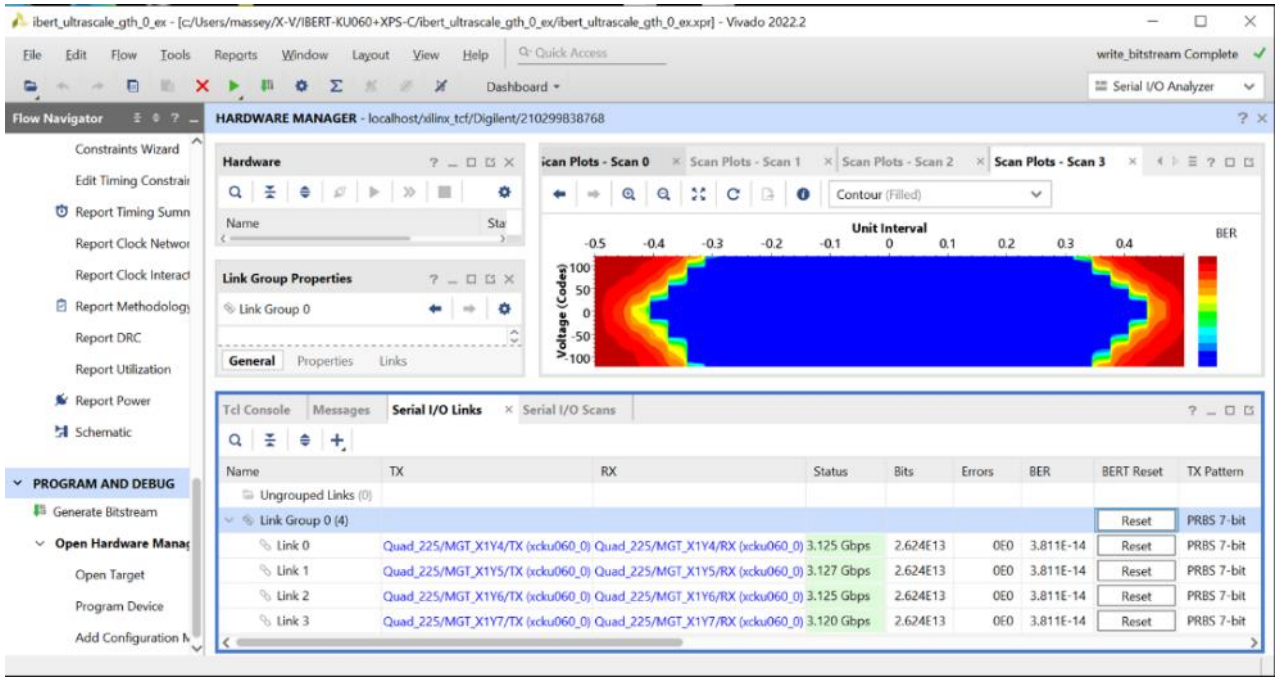

Figure 9: Xilinx Vivado IBERT Data Eye: XQRKU060 SERDES Quad 225 + UT65CML8X8FD XPS, Ch. 3 - BER

Summary & Conclusions

Vivado IBERT Loop-Back Test Measured Results:

Bit Error Rate (BER) =3.81e-14 for Limited Run Time (2.62e+13 Bits).

Desired BER ≤ 1e-12

Eye Opening = 84.85% UI