FRONTGRADE

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UT63M143
MIL-STD-1553A/Bus +3.3V Transceiver

Version #: 1.2.0

7/1/2019

Features

- 3.3-volt only operation
- Dual-cavity monolithic silicon technology
- Fit and functionally compatible to industry standard transceiver
- Idle low transmitter inputs and receiver outputs
- Operating temperature range: -55℃ to +125℃
- Operational environment:
  — Total-dose tolerance: 300 krads and 1Mrad(Si)
  — SEL Immune to a LET of 111 MeV-cm2/mg
- Packaging options:
  — 24-lead flatpack, dual-channel 50-mil center
  — 36-pin DIP, dual-channel 100-mil center
- Standard Microcircuit Drawing (SMD): 5962-07242
  — QML Q and QML V compliant part

Introduction

The monolithic UT63M143 Transceivers are complete transmitter and receiver pairs for +3-volt MIL-STD-1553A and 1553B applications. Encoder and decoder interfaces are idle low.

The receiver section of the UT63M143 series accepts biphase-modulated Manchester II bipolar data from a MIL- STD-1553 data bus and produces TTL-level signal data at its RXOUT and $\overline{RXOUT}$ outputs. An external RXEN input enables the receiver outputs or disables them low.

The transmitter section accepts biphase TTL-level signal data at its TXIN and $\overline{TXIN}$ and produces MIL-STD-1553 data signals. The transmitter's output voltage is typically 7.1 $V_{PP,LL}$. Activating the TXIHB input or setting both data inputs to the same logic level disables the transmitter outputs.

The UT63M143 series offers complete transmitter and receiver pairs packaged in a dual-channel 36-pin DIP or 24- lead flatpack configurations designed for use in any MIL-STD-1553 application.
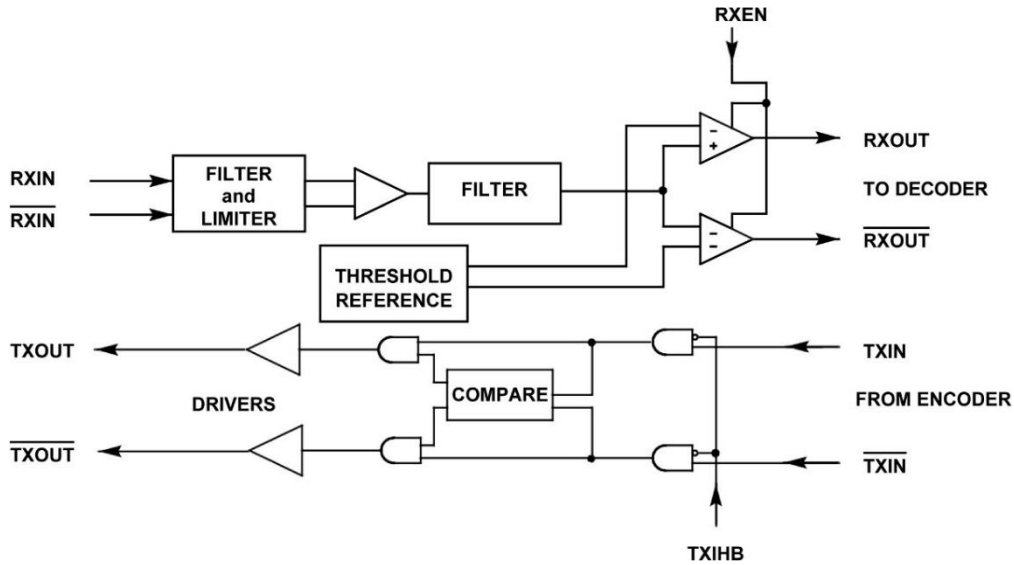
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Figure 1. Functional Block Diagram

Legend for TYPE field

- TI   TTL input
- TO   TTL output
- DO   Differential output
- DI   Differential input
- DIO   Differential input/output
- ( )   Channel designator
- [ ]   24-lead flatpack

Transmitter

Name	Pin Number	Type	Description
TXOUT [1] (A)	1 [1]	DO [DIO]	Transmitter outputs: TXOUT and $\overline{\text{TXOUT}}$ are differential data signals.
TXOUT (B)	10 [7]	DO [DIO]	
$\overline{\text{TXOUT}}$ [1] (A)	2 [2]	DO [DIO]	$\overline{\text{TXOUT}}$ is the half-cycle complement of TXOUT.
$\overline{\text{TXOUT}}$ (B)	11 [8]	DO [DIO]	

Name	Pin Number	Type	Description
TXIHB (A)	34 [22]	TI	Transmitter inhibit: This is an active high input signal. High input disables transmitter outputs.
TXIHB (B)	25 [16]	TI	
TXIN (A)	35 [23]	TI	Transmitter input: TXIN and $\overline{TXIN}$ are complementary TTL- level Manchester II encoder inputs.
TXIN (B)	26 [17]	TI	
$\overline{TXIN}$ (A)	36 [24]	TI	$\overline{TXIN}$ is the complement of TXIN input.
$\overline{TXIN}$ (B)	27 [18]	TI	

Note:

1. The 24-lead flatpack internally connects TXOUT to RXIN (CHA, CHB) and $\overline{TXOUT}$ to $\overline{RXIN}$ (CHA, CHB) for each channel.

Receiver

Name	Pin Number	Type	Description
RXOUT (A)	5 [4]	TO	Receiver outputs: RXOUT and $\overline{RXOUT}$ are complementary Manchester II decoder outputs.
RXOUT (B)	14 [10]	TO	
$\overline{RXOUT}$ (A)	8 [6]	TO	$\overline{RXOUT}$ is the complement of RXOUT output.
$\overline{RXOUT}$ (B)	17 [12]	TO	
RXEN (A)	6 [5]	TI	Receiver enable/disable: This is an active high input signal. Low input forces RXOUT and $\overline{RXOUT}$ low.
RXEN (B)	15 [11]	TI	
RXIN [1] (A)	29 [1]	DI [DIO]	Receiver input: RXIN and $\overline{RXIN}$ are biphase-modulated Manchester II bipolar inputs from MIL-STD-1553 data bus.
RXIN (B)	20 [7]	DI [DIO]	
$\overline{RXIN}$ [1] (A)	30 [2]	DI [DIO]	$\overline{RXIN}$ is the half-cycle complement of RXIN input.
$\overline{RXIN}$ (B)	21 [8]	DI [DIO]	

Note:

1. The 24-lead flatpack internally connects TXOUT to RXIN (CHA, CHB) and $\overline{TXOUT}$ to $\overline{RXIN}$ (CHA, CHB) for each channel.

Power and Ground (Note 1)

Name	Pin Number	Type	Description
V_{DD} (A)	33 [20]	PWR	+3.3 VDC power (±0.15V) Recommended decoupling capacitors: 1µF (tantalum) and 0.1µF (ceramic)
V_{DD} (B)	24 [14]	PWR	
GND (A)	3, 7, 31 [3,19,21]	GND	Ground reference
GND (B)	12, 16, 22 [9,13,15]	GND	

Note:

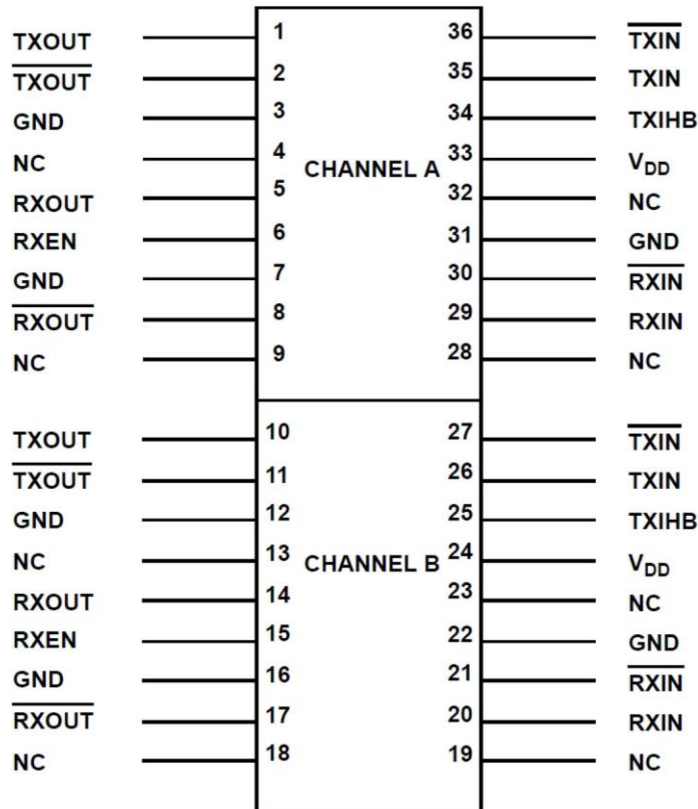1. Recommended decoupling it to place one 1µF Tantalum and one 0.1µF ceramic, capacitor as close as possible to each V_{DD} power pin.

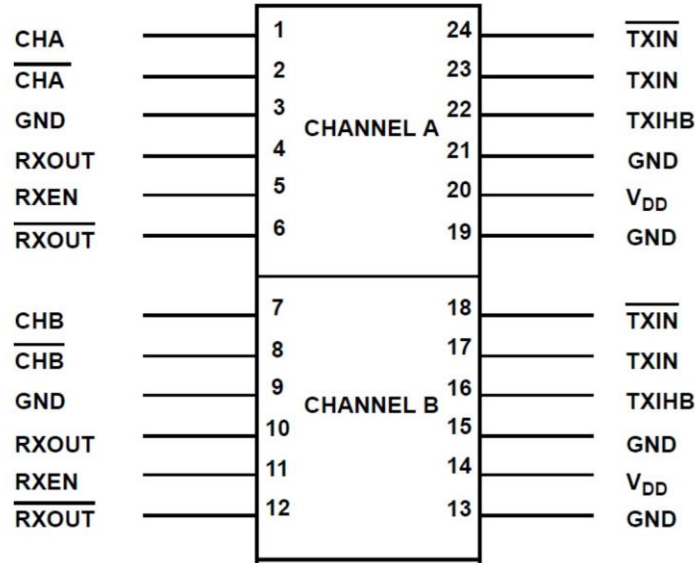Figure 2a. Functional Pin Diagram -- Dual Channel (36)

Figure 2b. Functional Pin Diagram -- Dual Channel (24) 1

Note:

1. The 24-lead flatpack internally connects TXOUT to RXIN (CHA, CHB) and TXOUT to RXIN (CHA, CHB) for each channel.

Transmitter

The transmitter section accepts TTL-level, biphase Manchester II encoded data and converts this data into differential phase-modulated current drive. The transmitter current drivers are coupled to a MIL-STD-1553 data bus via a transformer driven from the TXOUT and $\overline{\text{TXOUT}}$ terminals. The transmitter output terminals' non- transmitting state is enabled by asserting TXIHB (logic "1"), or by placing both TXIN and $\overline{\text{TXIN}}$ at the same logic level. Reference Table 1, Transmit Operating Mode, for a list of the functions for the output data in reference to the state of TXIHB. Figure 3 shows typical transmitter waveforms.

Receiver

The receiver section accepts biphase differential data from a MIL-STD-1553 data bus at its RXIN and $\overline{\text{RXIN}}$ inputs. The receiver converts input data to TTL-level, biphase Manchester II format and is available for decoding at the RXOUT and $\overline{\text{RXOUT}}$ terminals. The outputs RXOUT and $\overline{\text{RXOUT}}$ represent positive and negative excursions (respectively) of the inputs RXIN and $\overline{\text{RXIN}}$. Figure 4 shows typical receiver output waveforms.

Table 1. Transmit Operating Mode

TXIN	$\overline{\text{TXIN}}$	TXIHB	TXOUT
x[1]	x	1	OFF[2]
0	0	x	OFF[3]
0	1	0	ON
1	0	0	ON
1	1	x	OFF[3]

Notes:

1. x = Don't care.
2. Transmitter output terminals are in the non-transmitting mode during OFF-time.
3. Transmitter output terminals are in the non-transmitting mode during OFF-time, independent of TXIHB status.
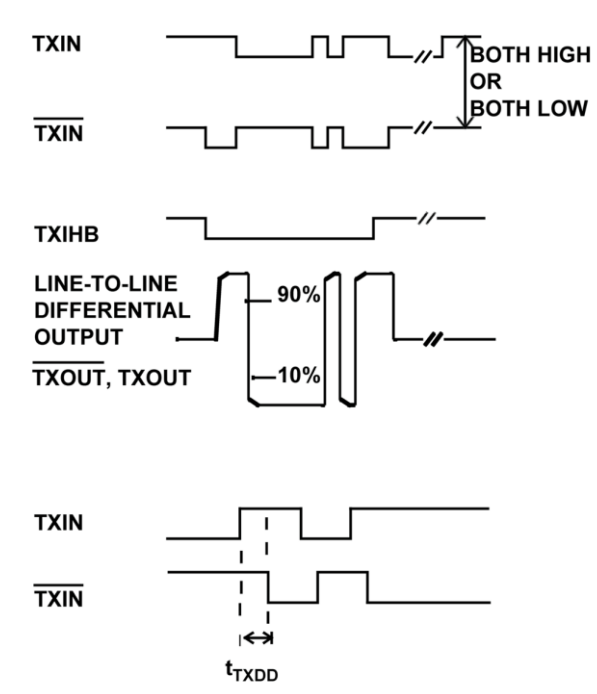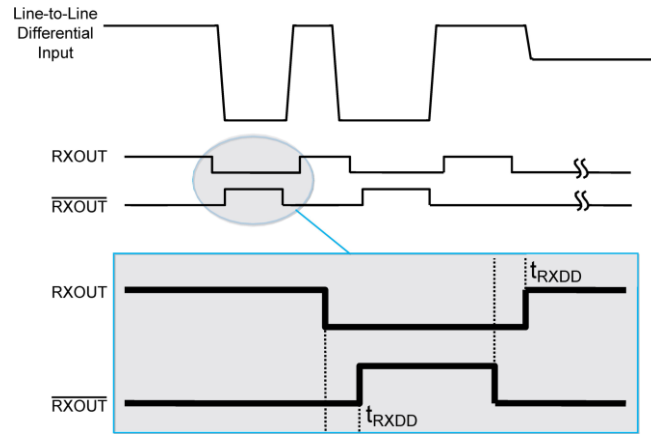

Figure 3. Typical Transmitter Wave

Figure 4. Typical Receiver Waveforms

Data Bus Interface [1]

The designer can connect the UT63M143 to the data bus via a short-stub (direct-coupling) connection or a long- stub (transformer-coupling) connection. Use a short-stub connection when the distance from the isolation transformer to the data bus does not exceed a one-foot maximum. Use a long-stub connection when the distance from the isolation transformer exceeds the one-foot maximum and is less than twenty feet. Figure 5 shows various examples of bus coupling configurations. The UT63M143 series transceivers are designed to function with MIL- STD-1553A and 1553B compatible transformers.

Note:

1. The 24-lead flatpack internally connects TXOUT to RXIN and $\overline{\text{TXOUT}}$ to $\overline{\text{RXIN}}$ for each channel.
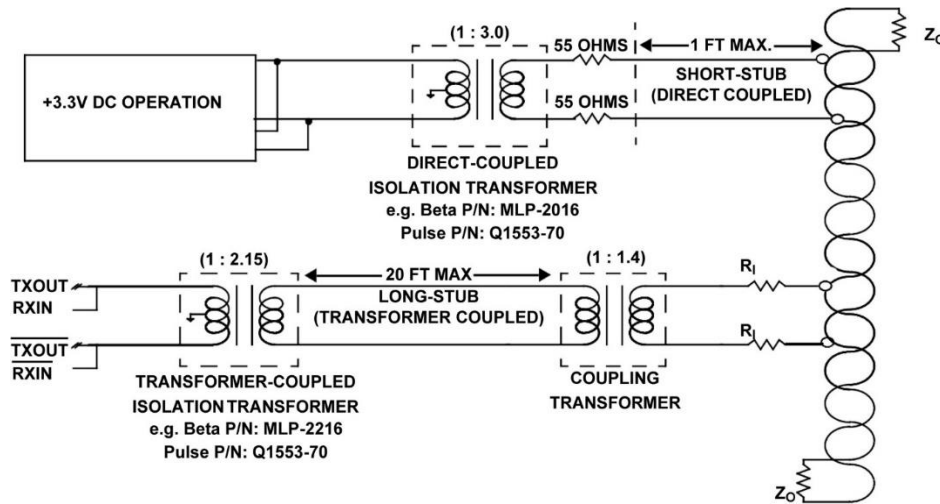
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Figure 5. Bus Coupling Configuration

Note:

1. The isolation resistor (R_I) is defined by MIL-STD-1553B, section 4.5.1.5.1.2 as equal to 0.75 x ZO ± 2%. Typically, 0.75x78Ω= 58.5Ω ⮕ ZO is the selected nominal cable impedance.
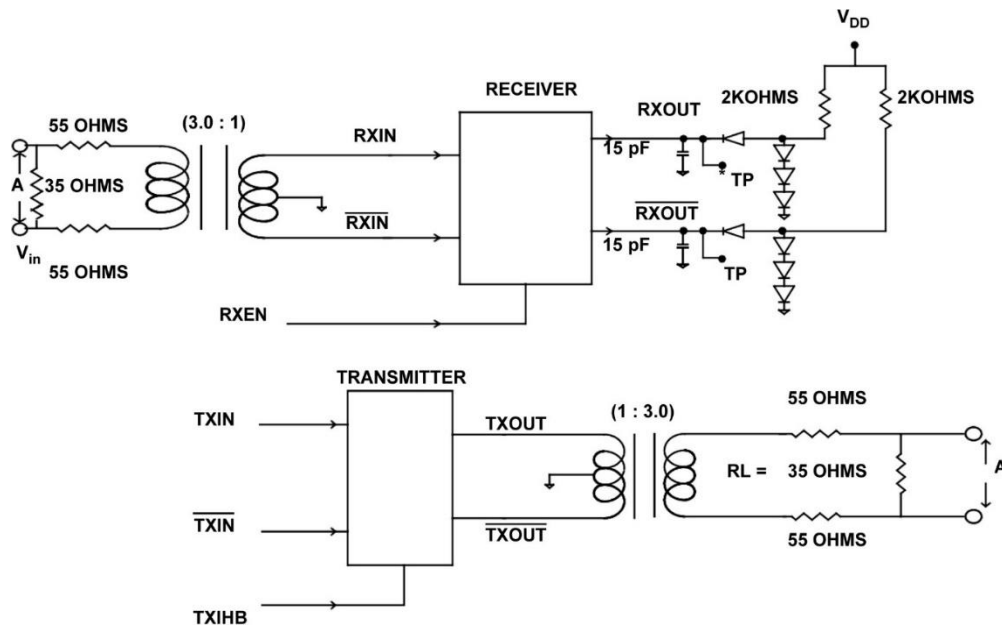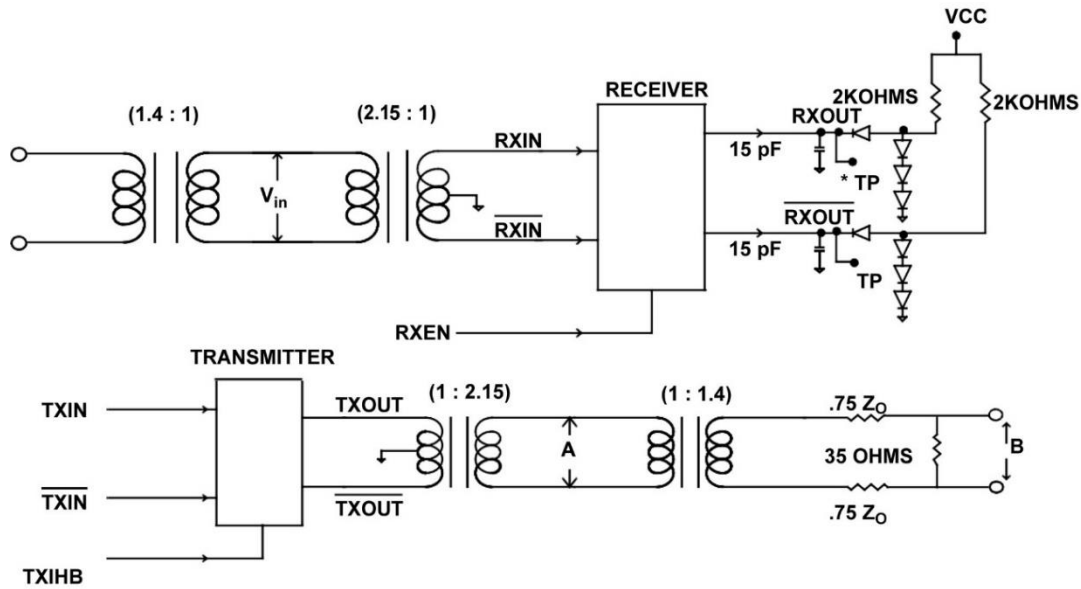

Figure 6. Direct Coupled Transceiver with Load

Notes:

1. TP = Test point.
2. RL removed for terminal input impedance test.

3. TXOUT and RXIN tied together. $\overline{\text{TXOUT}}$ and $\overline{\text{RXIN}}$ tied together.

Figure 7. Transformer Coupled Transceiver with Load

Notes:

1. TP = Test point.
2. RL removed for terminal impedance test.
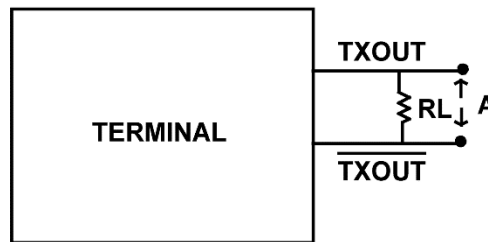3. $\overline{\text{TXOUT}}$ and $\overline{\text{RXIN}}$ tied together.

Figure 8. Transceiver Test Circuit MIL-STD-1553

Notes:

1. Transformer Coupled Stub: Terminal is defined as transceiver plus isolation transformer. Point A is defined in figure 7.
2. Direct Coupled Stub: Terminal is defined as transceiver plus isolation transformer and fault resistors. Point A is defined in figure 6.

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Table 2. Transformer Requirements

Coupling Technique	± 3.3VDC
DIRECT-COUPLED: Isolation Transformer Ratio	1 : 3.0
TRANSFORMER-COUPLED: Isolation Transformer Ratio	1 :2.15
Coupling Transformer Ratio	1 : 1.4

Recommended Thermal Protection

All packages should mount to or contact a heat removal rail located in the printed circuit board. To insure proper heat transfer between the package and the heat removal rail, use a thermally-conductive material between the package and the heat removal rail. A MIL-STD-883 TM5011 certified thermal bonding material, like AI Technologies ME7159, is a common thermal interface material for space applications.

Absolute Maximum Ratings [1]

Parameter	Limits	Unit
V_{DD}	-0.3 to +7.0	V
Input voltage range (receiver)[2]	8	VPP
Logic input voltage range	-0.3 to V_{DD} +0.3	V
Maximum Package Power dissipation @ Tc=+125℃[3]	7.1	W
3. Thermal impedance junction to case [3]	7.0	℃/W
Maximum junction temperature	+175	℃
Storage temperature	-65 to +150	℃
Receiver common mode input voltage range	-5 to +5	V

Notes:

1. Stress outside the listed absolute maximum rating may cause permanent damage to the devices. This is a stress rating only, and functional operation of the device at these or any other conditions beyond limits indicated in the operational sections of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Voltage measurements identified as Vpp, 1-1 are differential measurements. Voltage measurements identified as Vpp are single ended measurements with a ground reference.

3. $P_{DMAX} = (T_{JMAX} - T_{CMAX}) / Θ_{JC}$, per MIL-STD-883 M1012 Section 3.4.1

Recommended Operating Conditions

Parameter	Limits	Unit
Supply voltage range	+3.15 to +3.45	V
Logic input voltage range	0 to V_{DD}	V
Receiver differential voltage @ RXIN and $\overline{RXIN}$	0.4 to 3.0	$V_{P-P, L-L}$
Receiver common mode voltage range	±4.0	V
Driver peak output current	960	mA
Serial data rate	0.3 to 1	MHz
Case operating temperature range (T_C)	-55 to +125	℃
Driver typical output current	600	mA

Operational Environment

Parameter	Limits	Unit
Total Ionizing Dose	1E6	rads(Si)
Single Event Latchup Immune (SEL)	≤111	MeV-cm^2/mg

DC Electrical Characteristics [1]

(V_{DD} = 3.3V ±0.15V; -55℃ ≤ TC ≤ +125℃)

Symbol	Parameter	Minimum	Maximum	Unit	Condition
V_{IL}	Input low voltage		0.8	V	RXEN, TXIHB, TXIN, $\overline{TXIN}$
V_{IH}	Input high voltage	2.0		V	RXEN, TXIHB, TXIN, $\overline{TXIN}$
I_I	Input current	-10	10	µA	VIN = V_{DD} or VSS, RXEN2, TXIHB, TXIN, $\overline{TXIN}$
V_{OL}	Output low voltage		0.55	V	IOL = 4mA; RXOUT, $\overline{RXOUT}$
V_{OH}	Output high voltage	2.4		V	IOH = -0.4mA; RXOUT, $\overline{RXOUT}$
I_{DD}	V_{DD} supply current		14.5	mA	0% duty cycle (non-transmitting)
			200	mA	25% duty cycle (∫ = 1MHz)
			387	mA	50% duty cycle (∫ = 1MHz)
			670	mA	87.5% duty cycle (∫ = 1MHz)
			761	mA	100% duty cycle (∫ = 1MHz)3

Notes:

1. All tests guaranteed per test figure 6.
2. RXEN has ~1.2µA pull up.
3. Guaranteed by design but not tested.

Receiver Electrical Characteristics [1]

(V_{DD} = 3.3V ±0.15V; -55℃ ≤ TC ≤ +125℃)

Symbol	Parameter	Minimum	Maximum	Unit	Condition
C_{IN} [2]	Input capacitance		15	pF	RXEN, TXIHB TXIN, $\overline{TXIN}$; input ∫ = 1MHz @ 0V
C_{OUT} [2]	Output capacitance		20	pF	RXOUT, $\overline{RXOUT}$; ∫ = 1MHz @ 0V
V_{IC} [4]	Common mode input voltage	-5	5	V	Direct-coupled stub; input 1.2 VPP, 200ns rise/fall time ±25ns, ∫ = 1MHz
V_{TH}	Input threshold voltage[4] (no response)		0.20	$V_{PP,L-L}$	Transformer-coupled stub; input at ∫ = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)
	Input threshold voltage (no response)[6]		0.28	$V_{PP,L-L}$	Direct-coupled stub; input at ∫ = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)
	Input threshold voltage[4] (response)	0.86	14.0	$V_{PP,L-L}$	Transformer-coupled stub; input at ∫ = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)
	Input threshold voltage (response)[6]	1.2	20.0[5]	$V_{PP,L-L}$	Direct-coupled stub; input at ∫ = 1MHz, rise/fall time 200ns at (Receiver output 0 → 1 transition)
CMRR[3, 4]	Common mode rejection ratio	Pass/Fail		N/A	

Notes:

1. All tests guaranteed per test figure 6.
2. Guaranteed by device characterization. Capacitance is measured only for initial qualification and after any process or design changes which may affect input or output capacitance.
3. Pass/fail criteria per the test method described in MIL-HDBK-1553 Appendix A, RT Validation Test Plan, Section 5.1.2.2, Common Mode Rejection.
4. Guaranteed by design, but not tested.
5. Upper limit guaranteed by design, but not tested.
6. Tested functionally.

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Transmitter Electrical Characteristics [1]

(V$_{DD}$ = 3.3V ±0.15V; -55℃ ≤ TC ≤ +125℃)

Symbol	Parameter	MIN	MAX	Unit	Condition
V$_O$	Output voltage swing per MIL-STD-1553B [3, 5] (see figure 9)	18	27	V$_{PP,L-L}$	Transformer-coupled stub, Figure 8, Point A; input ∫ = 1MHz, RL = 70 ohms
	per MIL-STD-1553B (see figure 9)	6.0	9.0	V$_{PP,L-L}$	Direct-coupled stub, Figure 8, Point A; input ∫ = 1MHz, RL = 35 ohms
	per MIL-STD-1553A [5] (see figure 9)	6.0	20	V$_{PP,L-L}$	Figure 8, Point A; input ∫ = 1MHz, RL = 35 ohms
V$_{NS}$	Output noise voltage differential[5] (see figure 9)		14	mV-RMS$_{L-L}$	Transformer-coupled stub, Figure 8, Point A; input ∫ = DC to 10MHz, RL = 70 ohms
	Output noise voltage differential[2] (see figure 9)		5	mV-RMS$_{L-L}$	Direct-coupled stub, Figure 8, Point A; input ∫ = DC to 10MHz, RL = 35 ohms
V$_{OS}$	Output symmetry [5]	-250	+250	m$_{Vpeak,L-L}$	Transformer-coupled stub, Figure 8, Point A; RL = 140 ohms, measurement taken 2.5µs after end of transmission
	Output symmetry [4]	-90	+90	m$_{Vpeak,L-L}$	Direct-coupled stub, Figure 8, Point A; RL = 35 ohms, measurement taken 2.5µs after end of transmission
V$_{DIS}$	Output voltage distortion[5] (overshoot or ring) (see figure 9)	-900	+900	m$_{Vpeak,L-L}$	Transformer-coupled stub, Figure 8, Point A; RL = 70 ohms
	Output voltage distortion (overshoot or ring) (see figure 9)	-300	+300	m$_{Vpeak,L-L}$	Direct-coupled stub, Figure 8, Point A; RL = 35 ohms
C$_{IN}$ [6]	Input capacitance		15	pF	TXIHB, TXIN, TXIN; input ∫ = 1MHz @ 0V
T$_{IZ}$ [5]	Terminal input impedance	1		Kohm	Transformer-coupled stub, Figure 7, Point A; input ∫ = 75KHz to 1MHZ (power on or power off; non-transmitting, RL removed from circuit).
		2		Kohm	Direct-coupled stub, Figure 6, Point A; input ∫ = 75KHz to 1MHZ (power on or power off; non- transmitting, RL removed from circuit).

Notes:

1. All tests guaranteed per test figure 6.
2. Guaranteed by device characterization.
3. For MIL-STD-1760, 20VPP,L-L min. Tested in direct-coupled mode to limits of 6.67V to 9.0VPP,L-L.
4. Test in accordance with the method described in MIL-STD-1553B output symmetry, section 4.5.2.1.1.4.
5. Guaranteed by design, but not tested.
6. Guaranteed by device characterization. Capacitance is measured only for initial qualification and after any process or design changes which may affect input or output capacitance.

AC Electrical Characteristics 1

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(V$_{DD}$ = 3.3V ±0.15V; -55℃ ≤ TC ≤ +125℃)

Symbol	Parameter	Minimum	Maximum	Unit	Condition
t$_R$, t$_F$	Transmitter output rise/ fall time (see figure 10)	100	300	ns	Input ∫ = 1MHz 50% duty cycle: direct-coupled RL = 35 ohms output at 10% through 90% points TXOUT, $\overline{TXOUT}$. Figure 10.
t$_{RXDD}$	RXOUT delay	-200	200	ns	RXOUT to $\overline{RXOUT}$, Figure 4.
t$_{TXDD}$ [2]	TXIN skew	-25	25	ns	TXIN to$\overline{TXIN}$, Figure 3.
t$_{RZCD}$	Zero crossing distortion (see figure 11)	-150	150	ns	Direct-coupled stub; input ∫ = 1MHz, 3 VPP (skew INPUT ±150ns), rise/fall time 200ns.
t$_{TZCS}$	Zero crossing stability (see figure 10)	-25	25	ns	Input TXIN and $\overline{TXIN}$ should create Transmitter output zero crossings at 500ns, 1000ns, 1500ns, and 2000ns. These zero crossings should not deviate more than ±25ns.
t$_{DXOFF}$ [3]	Transmitter off; delay from inhibit active		100	ns	TXIN and TXIN toggling @ 1MHz; TXIHB transitions from logic zero to one, see figure 12.
t$_{DXON}$ [4]	Transmitter on; delay from inhibit inactive		150	ns	TXIN and $\overline{TXIN}$ toggling @ 1MHz; TXIHB transitions from logic one to zero, see figure 12.
t$_{RCVOFF}$	Receiver off		50	ns	Receiver turn off time, see figure 13.
t$_{RCVON}$	Receiver on		50	ns	Receiver turn on time, see figure 13.
t$_{RCVPD}$	Receiver propagation		450	ns	Receiver propagation delay, see figure 13.
t$_{XMITPD}$	Transmitter propagation		200	ns	Transmitter propagation delay, see figure 12.

Notes:

1. All tests guaranteed per test figure 6.
2. Supplied as a design limit but not guaranteed or tested.
3. Delay time from transmit inhibit (1.5V) rising to transmit off (280mV).
4. Delay time from not transmit inhibit (1.5V) falling to transmit on (1.2V).
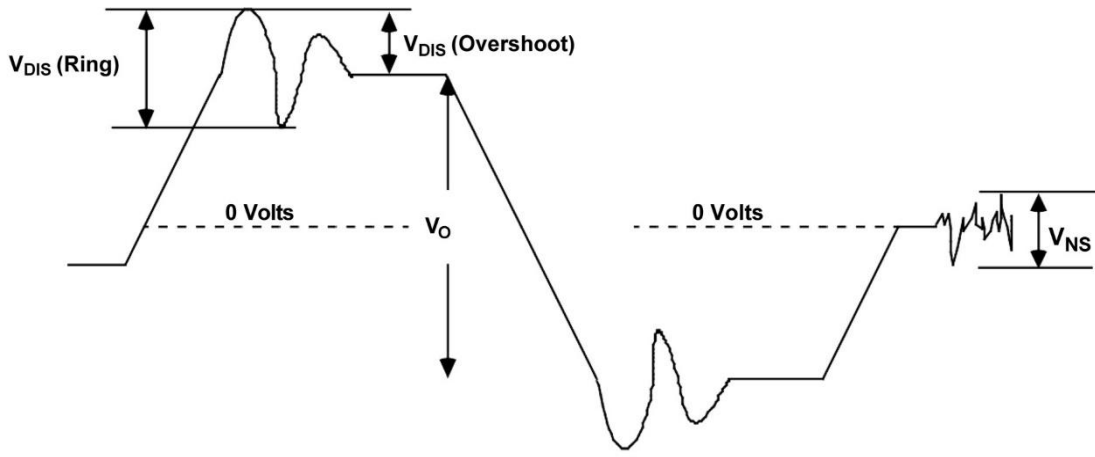
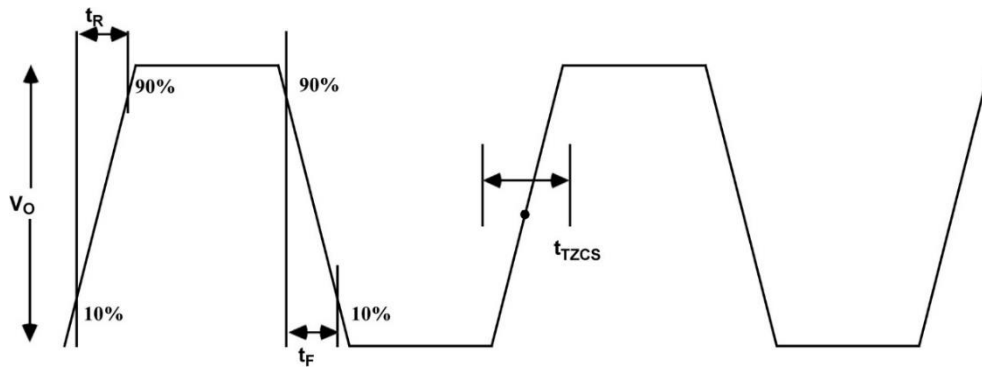Figure 9. Transmitter Output Characteristics (VDIS, VNS, VO)

Figure 10. Transmitter Output Zero Crossing Stability, Rise Time, Fall Time (tTZCS, tR, tF)

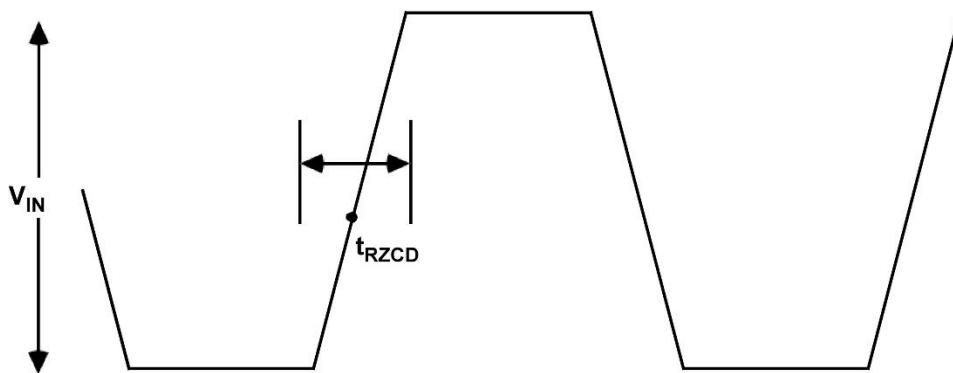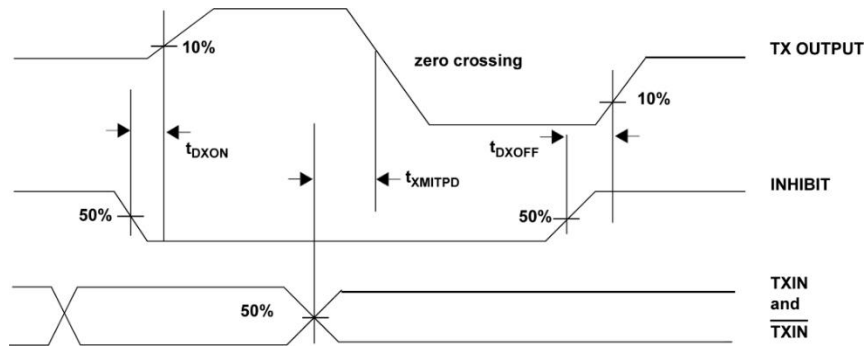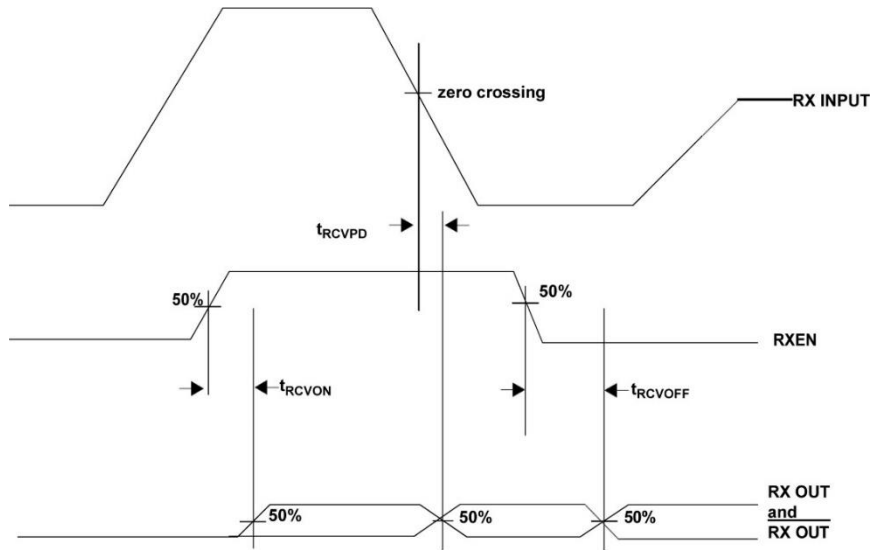Figure 11. Receiver Input Zero Crossing Distortion (tRZCD)

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Figure 12. Transmitter Timing
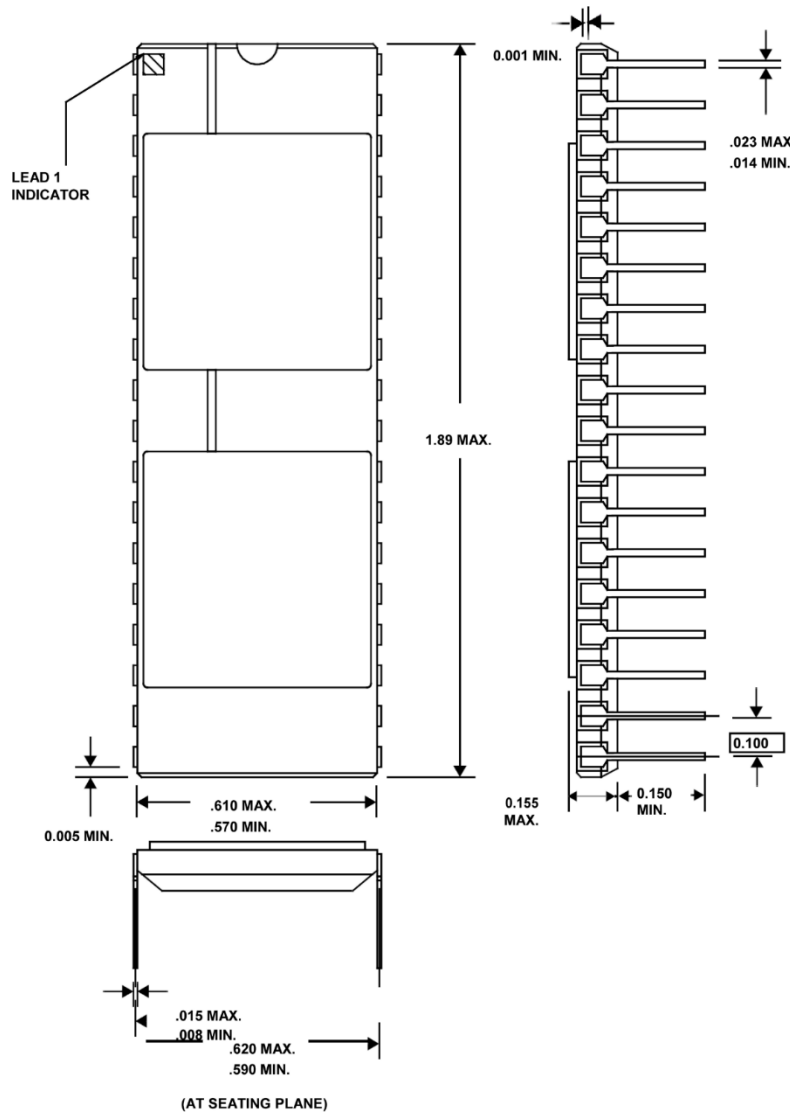

Figure 13. Receiver Timing

Figure 14. 36-Pin Side-Brazed DIP, Dual Cavity

Notes:

1. Package material: opaque ceramic.

2. All package finishes are per MIL-PRF-38535.

3. It is recommended that package ceramic be mounted on a heat removal rail in the printed circuit board. A thermally conductive material should be used.
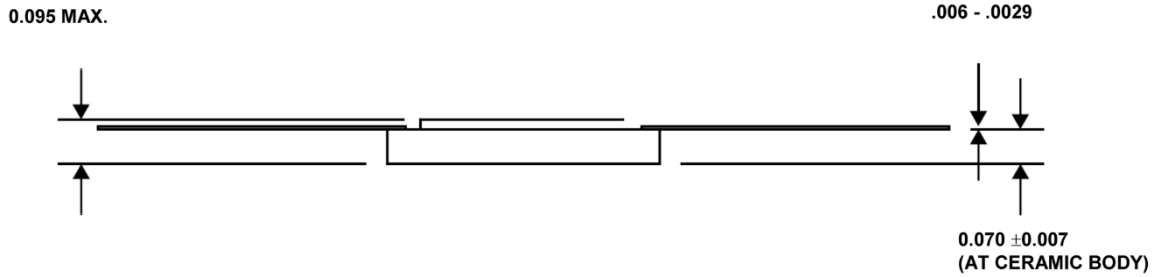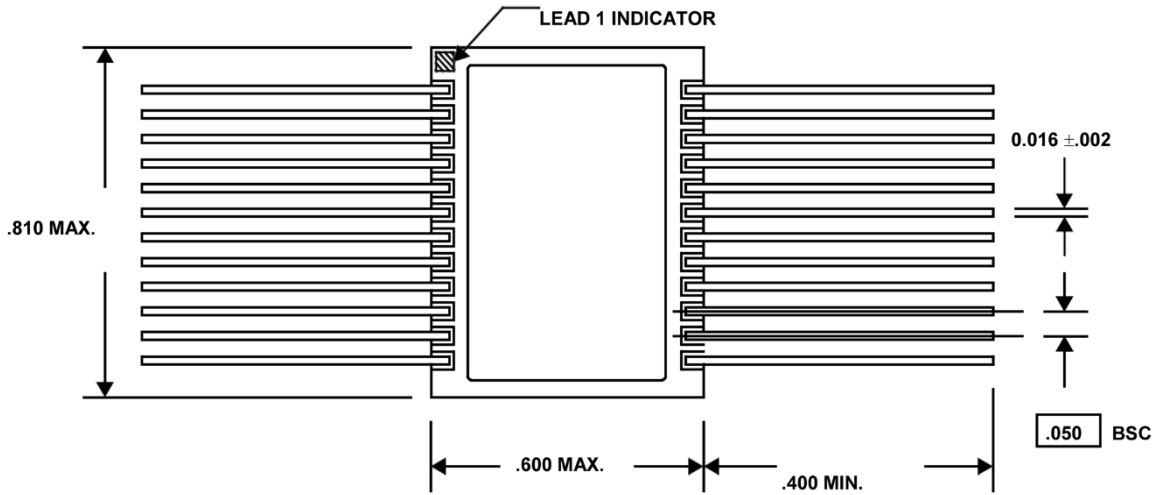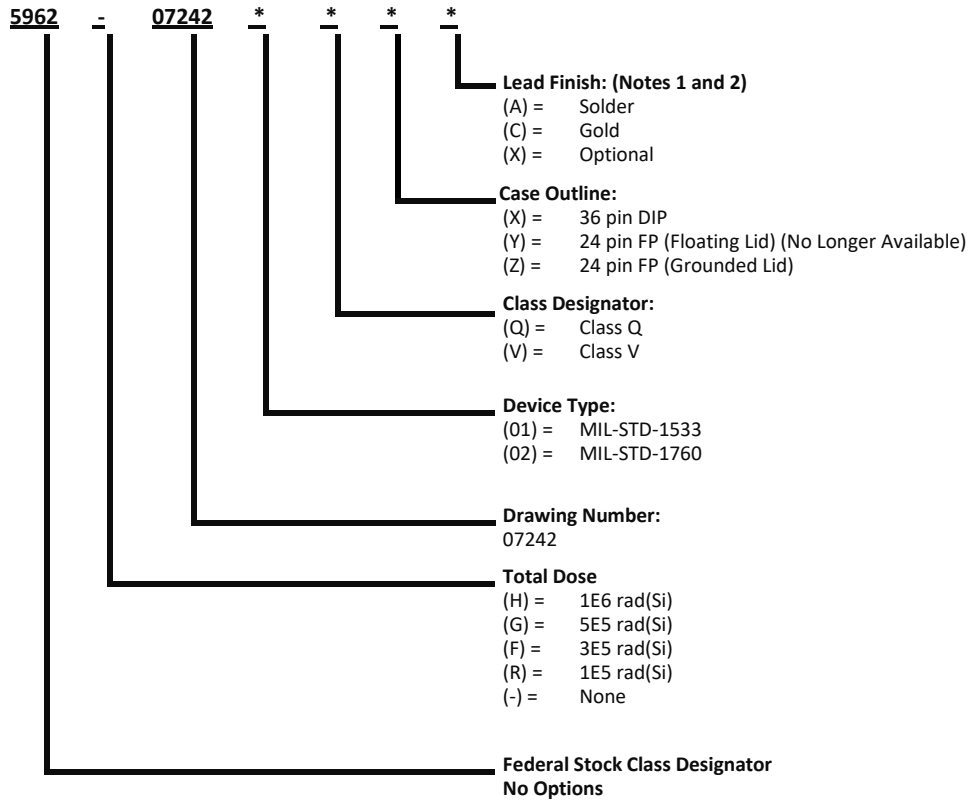
4. Units are in inches.

Figure 15. 24-Lead Flatpack, Top Brazed, Dual Cavity (50-mil lead spacing)

Notes:

1. Package material: opaque ceramic.
2. All package plating finishes are per MIL-PRF-38535.
3. It is recommended that package ceramic be mounted to a heat removal rail located in the printed circuit board. A thermally conductive material should be used.
4. Units are in inches.

Ordering Information

SMD Part Number Ordering Information

```
5962   -   07242   *   *   *   *
```

Lead Finish: (Notes 1 and 2)
(A) =   Solder
(C) =   Gold
(X) =   Optional

Case Outline:
(X) =   36 pin DIP
(Y) =   24 pin FP (Floating Lid) (No Longer Available)
(Z) =   24 pin FP (Grounded Lid)

Class Designator:
(Q) =   Class Q
(V) =   Class V

Device Type:
(01) =   MIL-STD-1533
(02) =   MIL-STD-1760

Drawing Number:
07242

Total Dose
(H) =   1E6 rad(Si)
(G) =   5E5 rad(Si)
(F) =   3E5 rad(Si)
(R) =   1E5 rad(Si)
(-) =   None

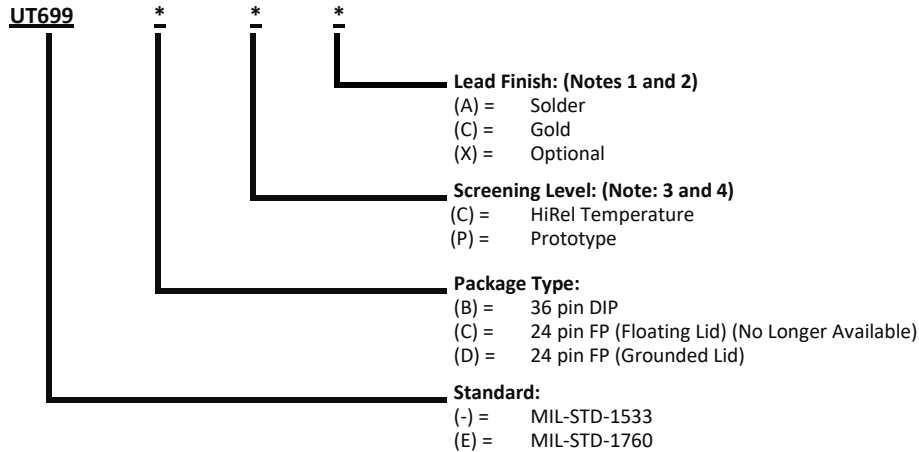**Federal Stock Class Designator**
No Options

Notes:

1. Lead finish (A, C, or X) must be specified.

2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

3. Total dose must be specified for all QML V devices.

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Ordering Information

Frontgrade Part Numbering Ordering Information

<u>UT699</u>   *   *   *

Lead Finish: (Notes 1 and 2)
(A) =   Solder
(C) =   Gold
(X) =   Optional

Screening Level: (Note: 3 and 4)
(C) =   HiRel Temperature
(P) =   Prototype

Package Type:
(B) =   36 pin DIP
(C) =   24 pin FP (Floating Lid) (No Longer Available)
(D) =   24 pin FP (Grounded Lid)

Standard:
(-) =   MIL-STD-1533
(E) =   MIL-STD-1760

Notes:

1. Lead finish (A, C, or X) must be specified.

2. If an "X" is specified when ordering, part marking will match the lead finish and will be either "A" (solder) or "C" (gold).

3. HiRel Temperature range devices are burned-in and tested at -55℃, room temperature, and 125℃. Radiation characteristics are neither tested nor guaranteed and may not be specified.

4. Prototype devices are tested at 25℃ only. Radiation characteristics are neither tested nor guaranteed and may not be specified. Lead finish is GOLD only.

Revision History

Date	Revision #	Author	Change Description	Page #
9-09	1.0.0		Last official release	
12-15	1.1.0		Updated Figure 4 Edited Table 2 and Absolute Maximums Applied new Frontgrade Data Sheet template Page 6 clarified Figure 4 Timing Diagrams Page 7: Corrected note for Figure 5 Page 8: Added "Point A" notation to Figure 6	p. 6, 8
7-19	1.2.0		Added 24-pin FP offering with grounded lid and obsoleted 24-pn FP offering with floating lid.	

Datasheet Definitions

	Definition
Advanced Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is still in the development stage and the **datasheet is subject to change**. Specifications can be **TBD** and the part package and pinout are **not final.**
Preliminary Datasheet	Frontgrade reserves the right to make changes to any products and services described herein at any time without notice. The product is in the characterization stage and prototypes are available.
Datasheet	Product is in production and any changes to the product and services described herein will follow a formal customer notification process for form, fit or function changes.