Command and Address Usage

Product Name	Manufacturer Part Number	SMD #	Device Type	Internal PIC Number
4M Asynchronous SRAM	UT8R128K32	5962-03236	All	WC03
4M Asynchronous SRAM	UT8R512K8	5962-03235	All	WC01
16M Asynchronous SRAM	UT8CR512K32	5962-04227	All	MQ08
16M Asynchronous SRAM	UT8ER512K32	5962-06261	All	WC04/05
4M Asynchronous SRAM	UT8Q512E	5962-99607	All	WJ02
4M Asynchronous SRAM	UT9Q512E	5962-00536	All	WJ01
16M Asynchronous SRAM	UT8Q512K32E	5962-01533	All	QS04
16M Asynchronous SRAM	UT9Q512K32E	5962-01511	All	QS03
32M Asynchronous SRAM	UT8ER1M32	5962-10202	All	QS16/17
64M Asynchronous SRAM	UT8ER2M32	5962-10203	All	QS09/10
128M Asynchronous SRAM	UT8ER4M32	5962-10204	All	QS11/12
40M Asynchronous SRAM	UT8R1M39	5962-10205	All	QS13
80M Asynchronous SRAM	UT8R2M39	5962-10206	All	QS14
160M Asynchronous SRAM	UT8R4M39	5962-10207	All	QS15

Overview

The purpose of this application note is to discuss how Frontgrade SRAMs perform a read and the ramifications to the system.

Read Cycle

The aforementioned Frontgrade designed SRAMs all employ an architecture which reduces power consumption during read accesses. The architecture internally senses data only when new data is requested. A request for new data occurs anytime the chip enable device pin is asserted, or any of the device address inputs transition states while the chip enable is asserted. A trigger is generated and sent to the sensing circuit anytime a request for new data is observed. Chip Enable ($\overline{CE}$) is asserted when the pin is pulsed low and disabled with the pin is held high.

So it's important to qualify when the trigger is generated (t=0). Basically $\overline{CE}$ assertion brings the device out of standby mode. When this happens the address decoders as well as all control inputs are turned on. Address transitions that occur previous to the device being enabled are moot.

When $\overline{CE}$ is low, t=0 occurs at the first address transition. If $\overline{CE}$ and addresses are transitioning simultaneously, t=0 is when $\overline{CE}$ reaches about 1.5V. All addresses should transition no later than 4ns from t=0. The sensitive time is if an address transitions between 4-7ns of t=0. If it is an address access and /CE has already been set up low, then all the address to address skew needs to be within 4ns. In this scenario t=0 is the first address to transition though its switching threshold. Errors observed from this are very rare in the range of single digits in millions of read requests; however, excessive overshoot and undershoot has been observed to make errors worse in this situation.

Besides sensitivity to address line skew, tying $\overline{CE}$ low can make the device more sensitive to system noise and non-monotonic edges. When $\overline{CE}$ is tied low, the part is actively 'listening' to the inputs of command pins as well as all the address lines. Any noise on the command or address pins while CE is tied low will be captured as a request to the memory. Non-monotonic edges on the command or address pins while CE is tied low can cause unintended

Command and Address Usage

requests to be interpreted by the memory chip. If there is an error due to skew or non-monotonic edges that occur during the 4-7ns window, the output will not change until a new read cycle is triggered by a change in inputs. Each read cycle is 7ns in length.

Skew between the CE and address signals will occur due to differences in loading. Consider the application where several SRAM devices are connected to the same memory bus. The address bus is commonly connected to all the devices, but the chip enable pin is singularly connected to each individual SRAM. This configuration results in a loading difference between the address inputs and the chip enable. This lightly loaded chip enable propagates to the memory more quickly than the heavily loaded address lines.

Simultaneous switching of controls and address inputs is not recommended for a couple of reasons. The first is the previously described signal skew sensitivity between controls and/or address inputs. The second reason is that activating all the controls and address inputs simultaneously results in peak instantaneous current consumption. This condition causes maximum strain to the power decoupling. Chip Enable activates address decoding circuits, address switching introduces input buffer switching current, and output enable assertion turns on all the device output drivers. Performing all three simultaneously results in worst case transient current demand by the memory. Proper decoupling between VDD and GND is necessary for simultaneous signal control and address signal changes.

Although errors from these conditions are very rare, the space environment requires as close to zero errors as possible. To avoid issues from these cases, Frontgrade recommends not tying $\overline{CE}$ low on a permanent basis and, toggling $\overline{CE}$ low after command and address signals are stable to capture the intended request to the memory chip. Also, bring $\overline{CE}$ back high before transitioning the command address signals. If there are no concerns with skew or noise, then Output Enable and address control are acceptable methods.

Command and Address Usage

App Note Revision History

Revision Date	Description of Change	Page(s)	Author
6/23	Initial Release	All	Nelson

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.

FRONTGRADE
APPLICATION NOTE
RELEASED 03/23