IBIS-AMI Model for the UT65CML8X8FD 3.125Gbps Crosspoint Switch

PRODUCT NAME	MANUFACTURER PART NUMBER	SMD #	DEVICE TYPE	INTERNAL PIC NUMBER
3.125Gbps 8 X 8 CROSSPOINT SWITCH	UT65CML8X8FD	5962-17213	01	WQ04

Table 1: Cross Reference of Applicable Products

1.0   Overview

CAES is developing a 3.125Gbps per channel 8 x 8, Full Duplex Crosspoint Switch Matrix with the aim of supporting the emerging VITA78 Space VPX standard and its specifications for a data plane switch function enabling a redundant and cross-strapped serial data path within the VPX chassis. The Current Mode Logic (CML) transmitter and receiver input-output (IO) buffers on the crosspoint switch implement high-speed signal conditioning features such as transmit drive current level adjustment and receive signal continuous time linear equalization (CTLE). In order to enable Electronic Design Automation (EDA) simulations validating the customer applications of the UT65CML8X8FD, CAES developed an Input/output Buffer Information Specification Algorithmic Modeling Interface model (IBIS-AMI), for use in 64-bit Microsoft Windows channel simulator software tools. The initial release of the UT65CML8X8FD IBIS- AMI model supports only the typical process, voltage and temperature (PVT) corner – typical wafer fabrication process, nominal power supply voltages and nominal (25°C) device junction temperature.

2.0   UT65CML8X8FD IBIS-AMI Model Description

The UT65CML8X8FD IBIS-AMI model is implemented in two separate model files and associated 64- bit Microsoft Windows dynamic linked libraries (DLLs) – TXCML18.ibs and TXCML18_x64.dll for the transmitter CML output buffer and RXCML12.ibs and RXCML12_x64.dll for the receiver CML input buffer, respectively. The folder location of these files should be the same as the simulation model project files, or it should be explicitly declared in the model source directory setup of the channel simulator software. These model files are assigned to individual IO buffer elements and cannot be assigned to Integrated Circuit (IC) objects within the channel simulator model setup. Figure 1 illustrates the IO buffer IBIS file assignment as shown in an example Free Form Schematic (FFS) simulation setup in Mentor Graphics HyperLynx channel simulator, using S-parameter files to model the transmission channel. The transmit and receive IBIS-AMI models of the UT65CML8X8FD crosspoint switch are of differential type and can only be assigned to differential buffer elements.
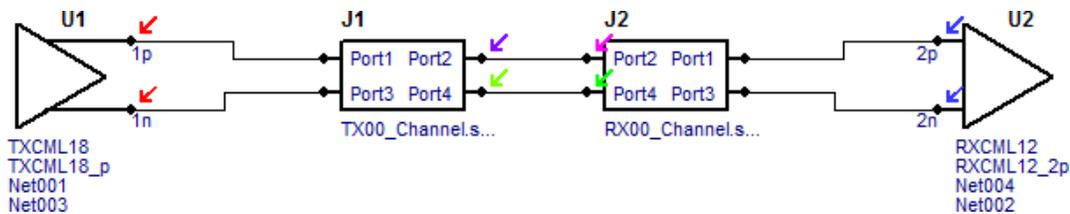

Figure 1: Mentor Graphics HyperLynx FFS schematic example

IBIS-AMI Model for the UT65CML8X8FD 3.125Gbps Crosspoint Switch

2.1 UT65CML8X8FD TXCML18 IBIS-AMI Model Description

The UT65CML8X8FD TXCML18 model file contains two user-controlled variables – *OutputGain* (always set to 1) and *txi* set in the range of decimal 0 to 15. The *txi* variable provides the user the ability to model the CML transmitter output signal amplitude at the die pad with varying drive current strength settings in the range of binary 4'b0000 to 4'b1111 of the TX_I_n<m> 4-bit drive strength register. The *txi*=0 (4'b0000) setting corresponds to the lowest amplitude setting, while the *txi*=15 (4'b1111) corresponds to the highest amplitude setting of the TXCML output driver. The n<m> label denotes the transmit bank number and lane number of the device set of 32 transmit channels.

For more information on the UT65CML8X8FD transmitter drive current settings, refer to the device datasheet.

Figure 2 shows an example of the TXCML18 IBIS-AMI model user-controlled variable settings in Mentor Graphics HyperLynx channel simulator.
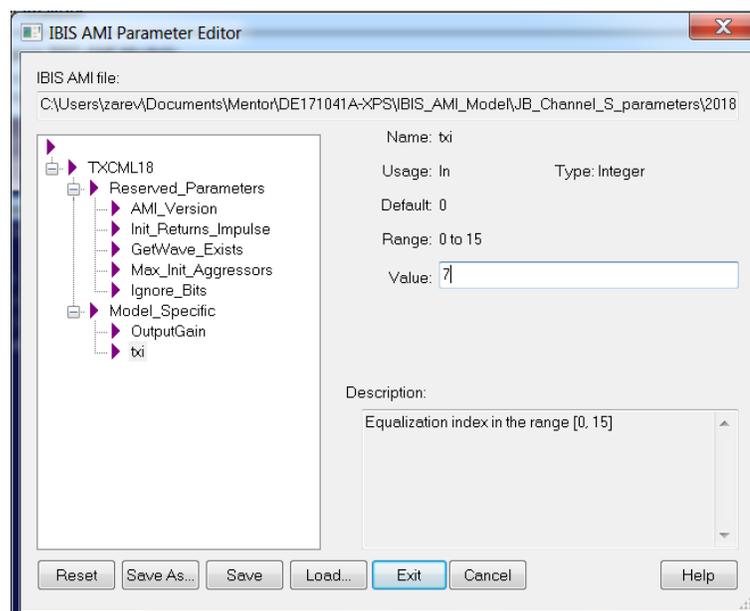

Figure 2: TX18CML IBIS-AMI model-specific user variables

It is to be noted that the transmitter output signal waveforms used in the txi variable settings, were produced using step response simulations and have been partially correlated to characterization data.

IBIS-AMI Model for the UT65CML8X8FD 3.125Gbps Crosspoint Switch

Figure 3 depicts the TXCML18 output buffer step response simulation results, used in the transmitter driver strength data set.
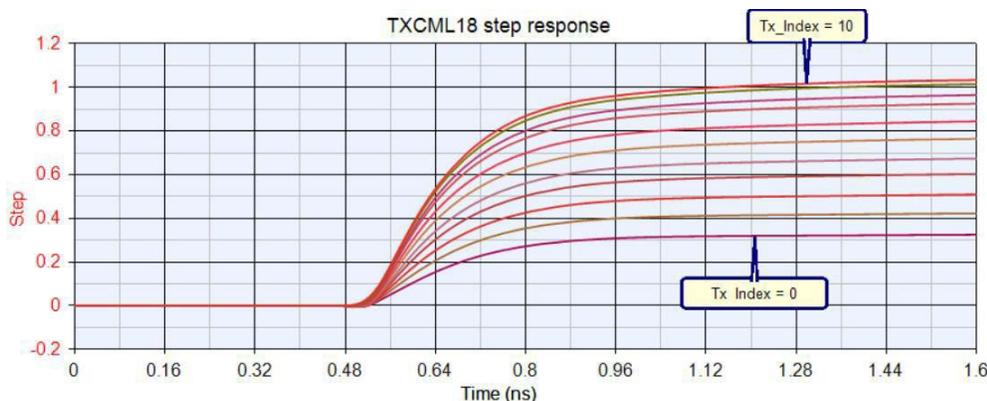

Figure 3: TXCML18 Step Response Simulation Results

2.2   UT65CML8X8FD RXCML18 IBIS-AMI Model Description

The UT65CML8X8FD RXCML18 IBIS-AMI model file contains three user-controlled variables – *InputGain* (always set to 1), *AutoInit* set to either 0 or 1 and *seq* set in the range of decimal 0 to 31. The *seq* variable provides the user the ability to model the CML receiver signal at the receiver internal die pad, with varying CTLE equalizer settings, in the range of binary 5'b00000 to 5'b11111 of the EQ_J_k<l> 5-bit receiver post-equalization register. The *seq*=0 (5'b00000) setting corresponds to the lowest equalizer setting, while the *seq*=31 (5'b11111) corresponds to the highest equalizer setting of the receiver variable gain amplifier. The J_k<l> label denotes the receiver bank number and lane number of the device set of 32 receive channels.

For more information on the UT65CML8X8FD receiver CTLE equalizer register settings, refer to the device datasheet. It is to be noted that with the *AutoInit* variable is set to 1, the user can perform a channel simulation that automatically selects the most optimal *seq* equalizer setting from the set of 32, for the given channel frequency loss profile. Figure 4 illustrates the user-controlled variables of the UT65CML8X8FD RXCML12 IBIS-AMI model file in the Mentor Graphics HyperLynx channel simulator.

Similarly to the TXCML18 IBIS-AMI model dataset, the RXCML12 IBIS-AMI model dataset was obtained by the means of step response simulations for all receiver equalizer settings in the range of decimal 0 to 31. Figure 5 illustrates the step response simulation results of the CTLE settings for *seq* = 0 to 15. As seen in the step response results, the higher index settings of the equalizer provide for signal peaking at the higher frequencies, at the expense of the lower frequency content of the receive signal frequency spectrum.

IBIS-AMI Model for the UT65CML8X8FD 3.125Gbps Crosspoint Switch
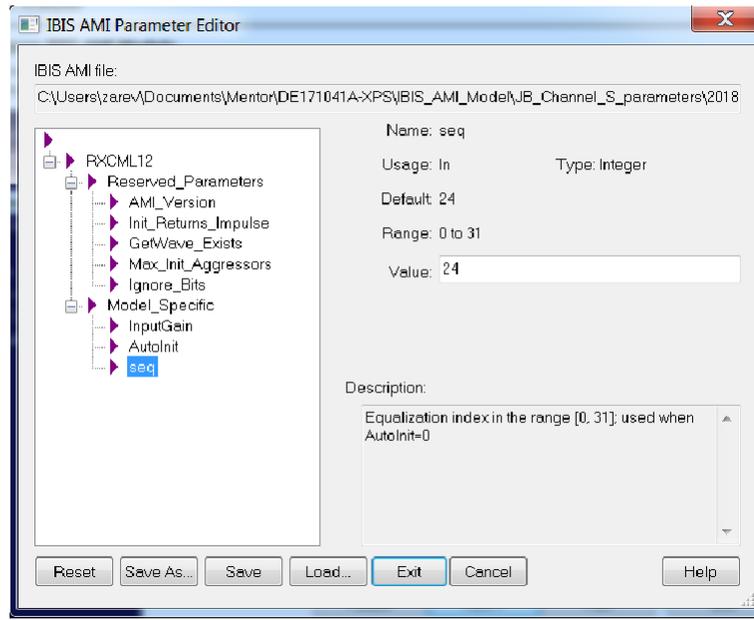
Figure 4: RX18CML IBIS-AMI model-specific user variables

This signal conditioning effect is also evident in the equivalent frequency response plot of the CTLE step response results shown in Figure 5.
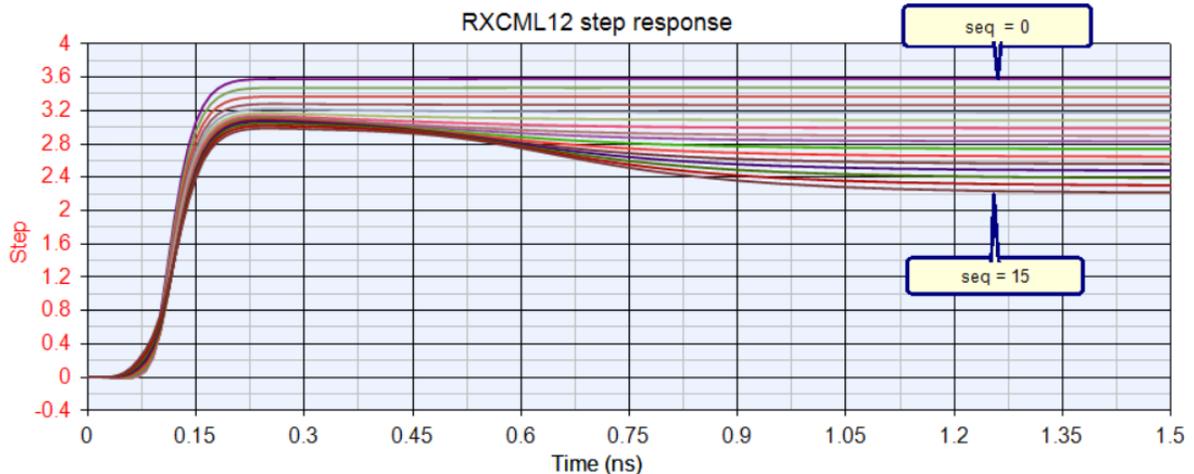

Figure 5: RXCML12 IBIS-AMI Model Step Response Results

As seen in Figure 6, best equalizer signal compensation results are accomplished with *seq* index settings that provide the optimal delta in [dBV] of the peaking frequency vs. the low frequency amplification for a given channel loss in [dB] at the signal line rate frequency.
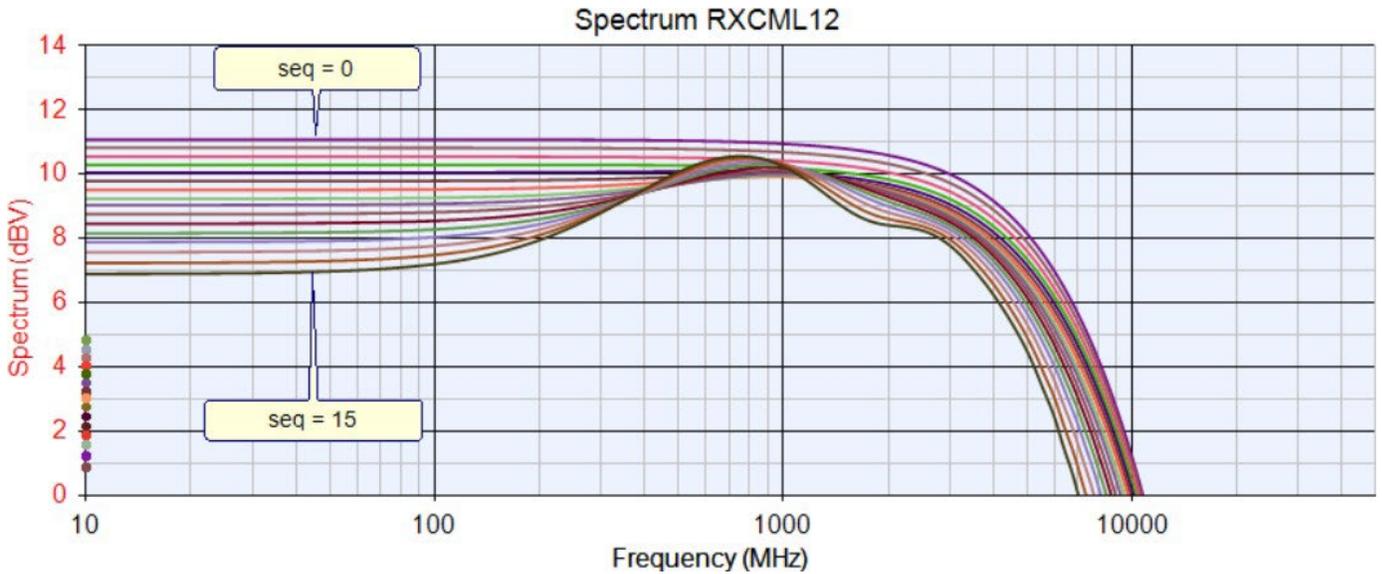
Figure 6: RXCML12 CTLE Frequency Responses

3.0   UT65CML8X8FD IBIS-AMI Model Verification and Result Correlation

The UT65CML8X8FD TX/RX IBIS-AMI Model verification was performed in two stages. The first stage used only the TXCML18 model and attempted to correlate its simulation results obtained from an equivalent S-parameter model simulation setup, with N4903B jBERT measurement results performed on the actual lab measurement setup. The second stage used an actual channel S-parameter model (shown in Figure 1), which was also derived from a lab measurement setup and attempted to correlate the simulation results using both the TXCML18 and the RXCML12 IBIS-AMI models between two independent channel simulators.

Figure 7 shows the HyperLynx simulation model setup for the TXCML18 IBIS-AMI model verification.
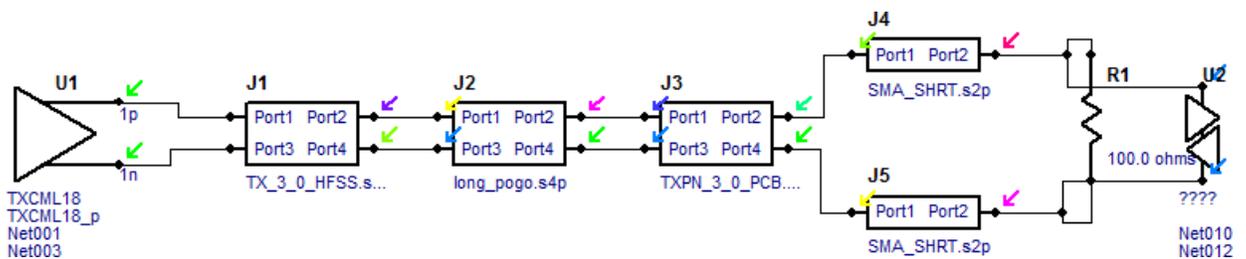

Figure 7: TXCML18 IBIS-AMI Model Verification Setup

IBIS-AMI Model for the UT65CML8X8FD 3.125Gbps Crosspoint Switch

Figure 8 shows the comparison of the simulation results obtained with the model in Figure 7 and the N4903B jBERT eye diagram measurement of the actual lab measurement test setup. As seen in Figure 8, the simulated and the measured eye diagrams are in very good general agreement as denoted by the eye height and eye width measurement parameters (simulated Eye Height = 440mV vs. measured Eye Height = 502mV and simulated Eye Width = 0.7885UI or 252ps vs. measured Eye Width =268ps).
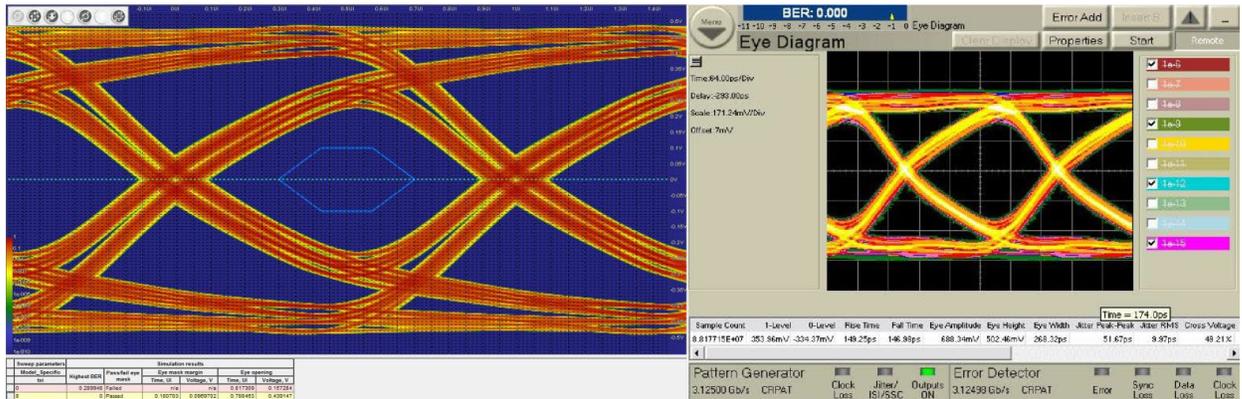
Figure 8: TXCML18 IBIS-AMI Model Simulated vs. Measured Eye Diagrams

Figure 9 illustrates the comparison of the simulated eye diagrams obtained from the model setup shown in Figure 1 with a simulated signal probe placed at the input the RXCML12 receive buffer prior to CTLE equalization, for two different channel simulators – HyperLynx and third party. As seen in Figure 9, both channel simulators provide nearly identical eye diagram results for the same simulation setup conditions of the channel model shown in Figure 1.
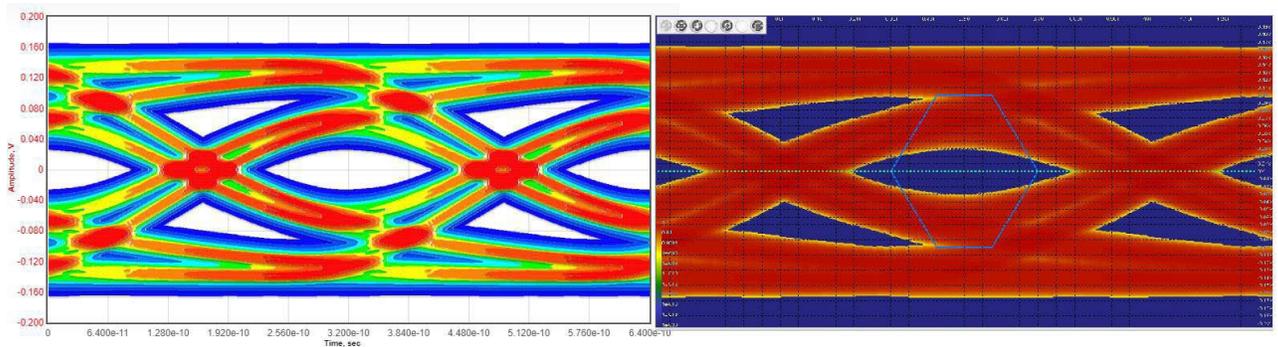

**Figure 9: IBIS-AMI Model Channel Simulator Comparison prior to CTLE**

IBIS-AMI Model for the UT65CML8X8FD 3.125Gbps Crosspoint Switch
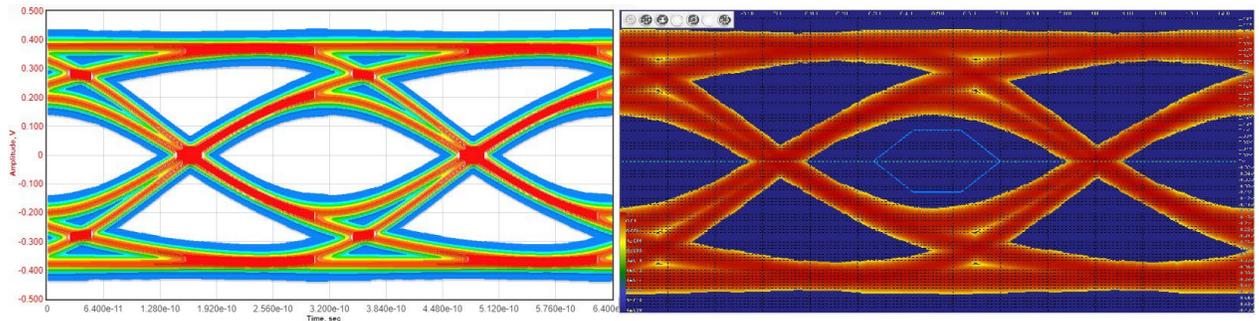
Figure 10: IBIS-AMI Model Channel Simulator Comparison after CTLE *seq*=11

Figure 10 shows the comparison of the eye diagram simulation results between the two channel simulators (HyperLynx and third party) with the user variable *AutoInit*=1 for the RXCML12 model and the auto selected *seq*=11 equalizer index. As seen in the figure, both channel simulators provide nearly identical simulated eye diagrams at the output of the receive equalization amplifier.

4.0   Summary and Conclusions

In summary and based on the UT65CML8X8FD IBIS-AMI model analysis using simulation result correlation between simulations and lab measurements as well as simulations comparison between two independent channel simulators, we conclude that the preliminary release of the UT65CML8X8FD IBIS-AMI model is valid and available for use in customer applications utilizing the high-speed signal conditioning capabilities of the device.

As noted in the overview, this preliminary IBIS-AMI model release is applicable only for the Typical PVT simulation corner for the device. The adjustable transmit and receive terminations on CML IO buffers were set at the most optimal value of 96Ohms. This value was used during the transmit and receive step response simulations that provided the basis for the TXCML18 and RXCML12 IBIS AMI datasets.

In addition to the UT65CML8X8FD IBIS-AMI model CAES also provides a full set of high-speed S-parameter models for all 32 transmit and receive differential pairs of the device package, as the TXCML18 and the RXCML12 model datasets do not contain any package parasitic parameters. The device package S-parameter dataset in conjunction with the TXCML18 and the RXCML12 IBIS-AMI models, provide for the most accurate user simulation models and results.

## 5.0   Appendix – A: Transmitter and Receiver Step Response Plots
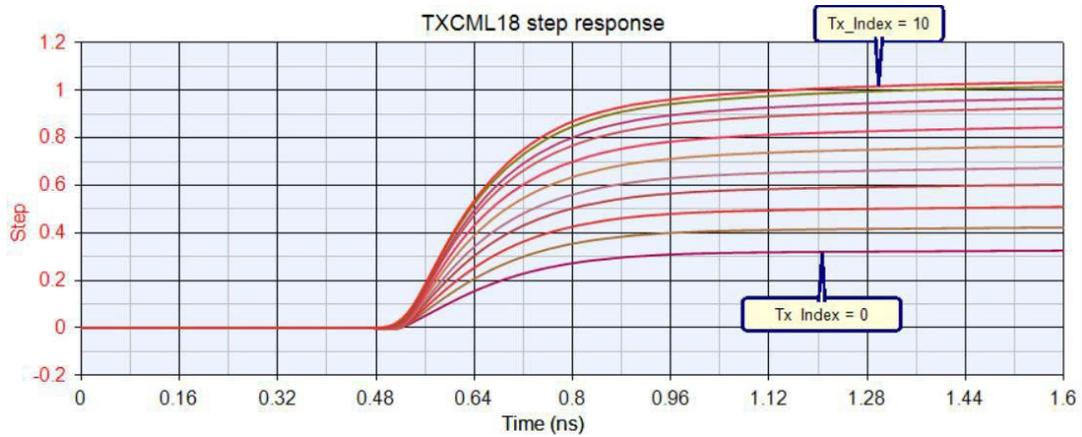

Figure 11: TXCML18 Step Response *txi* **= 0-10**
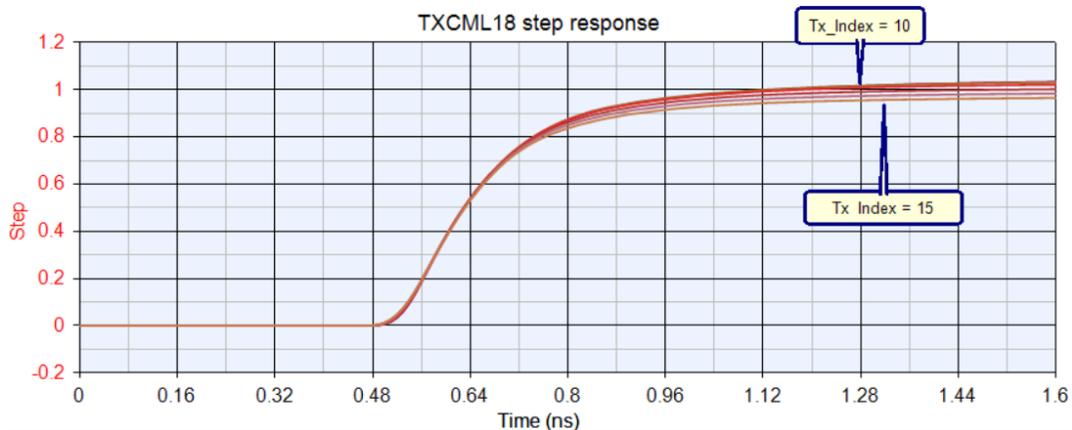

Figure 12: TXCML18 Step Response *txi* **= 10-15**
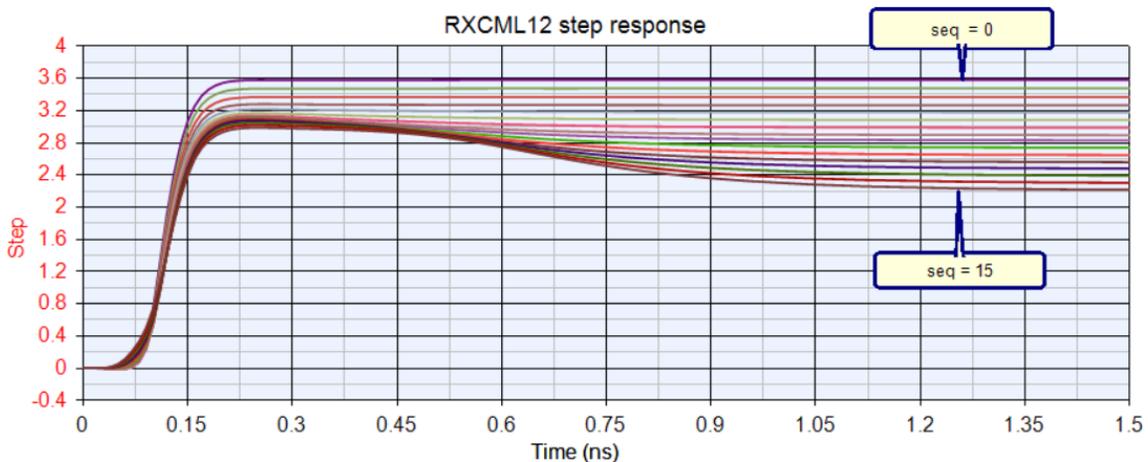
Figure 13: RXCML12 Step Response *seq* **= 0-15**

# IBIS-AMI Model for the UT65CML8X8FD 3.125Gbps Crosspoint Switch
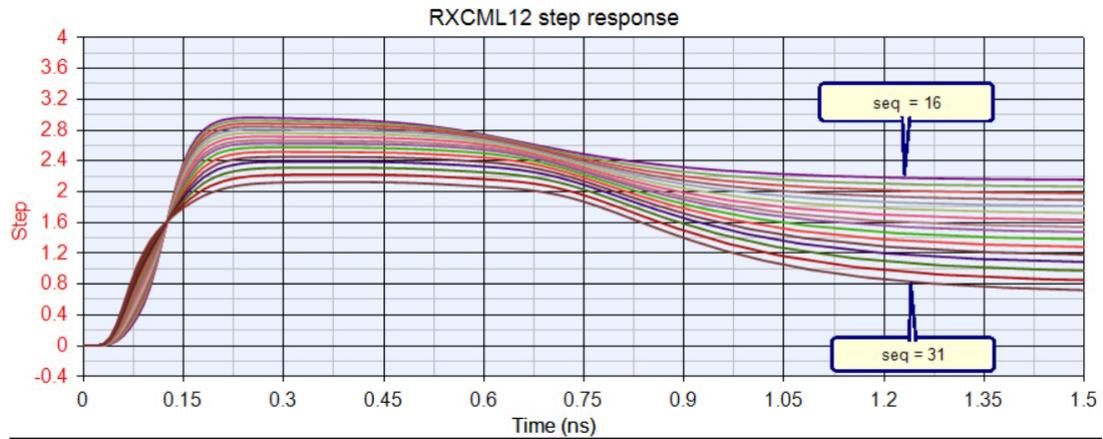
Figure 14: RXCML12 Step Response *seq* **= 16-31**
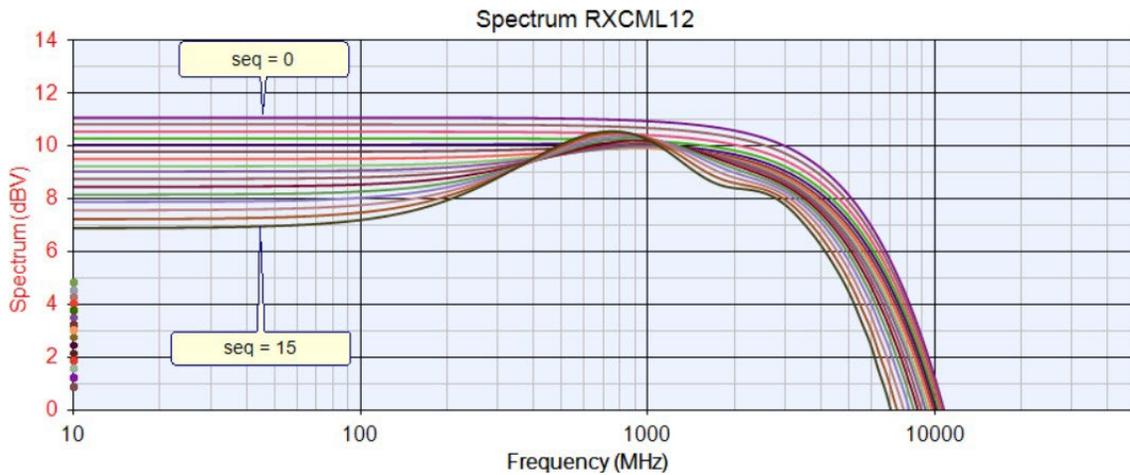
Figure 15: RXCML12 Frequency Response *seq* **= 0-15**
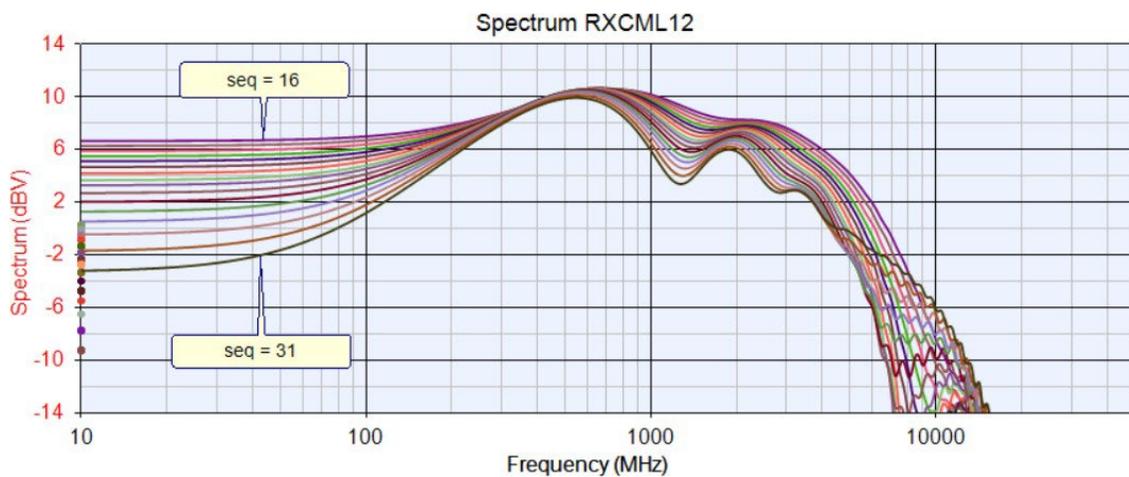
Figure 16: RXCML12 Frequency Response *seq* **= 16-31**

IBIS-AMI Model for the UT65CML8X8FD 3.125Gbps Crosspoint Switch

REVISION HISTORY

Date	Rev. #	Author	Change Description
06/08/2018	1.0.0	SZ	Initial Release

The following United States (U.S.) Department of Commerce statement shall be applicable if these commodities, technology, or software are exported from the U.S.: These commodities, technology, or software were exported from the United States in accordance with the Export Administration Regulations. Diversion contrary to U.S. law is prohibited.